SiT3521

PRELIMINARY

1 to 340 MHz Elite Platform™ I²C/SPI Programmable Oscillator

Description

The SiT3521 is an ultra-low jitter, user programmable oscillator which offers the system designer great flexibility and functionality.

The device supports two in-system programming options after powering up at a default, factory programmed startup frequency:

- Any-frequency mode where the clock output can be re-programmed to any frequency between 1 MHz and 340 MHz in 1 Hz steps
- Digitally controlled oscillator (DCO) mode where the clock output can be steered or pulled by up to ±3200 ppm with 5 to 94 ppt (parts per trillion) resolution.

The device's default start-up frequency is specified in the ordering code. User programming of the device is achieved via I²C or SPI. Up to 16 I²C addresses can be specified by the user either as a factory programmable option or via hardware pins, enabling the device to share the I²C with other I²C devices.

The SiT3521 utilizes SiTime's unique DualMEMS™ temperature sensing and TurboCompensation™ technology to deliver exceptional dynamic performance:

- Resistant to airflow and thermal shock
- Resistant to shock and vibration
- Superior power supply noise rejection

Combined with wide frequency range and user programmability, this device is ideal for telecom, networking and industrial applications that require a variety of frequencies and operate in noisy environment.

Features

- Programmable frequencies (factory or via I²C/SPI) from 1 MHz to 340 MHz
- Digital frequency pulling (DCO) via I²C/SPI
  - Output frequency pulling with perfect pull linearity
  - 13 programmable pull range options to ±3200 ppm
  - Frequency pull resolution as low as 5 ppt (0.005 ppb)
- 0.21 ps typical integrated phase jitter (12 kHz to 20 MHz)
- Integrated LDO for on-chip power supply noise filtering
- 0.02 ps/mV PSNR
- -40°C to 105°C operating temperature
- LVPECL, LVDS, or HCSL outputs
  - Programmable LVPECL, LVDS Swing
  - LVDS Common Mode Voltage Control
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

Applications

- Ethernet: 1/10/40/100/400 Gbps
- G.fast and xDSL
- Optical Transport: SONET/SDH, OTN
- Clock and data recovery
- Processor over-clocking
- Low jitter clock generation
- Server, storage, datacenter
- Test and measurement
- Broadcasting

Block Diagram

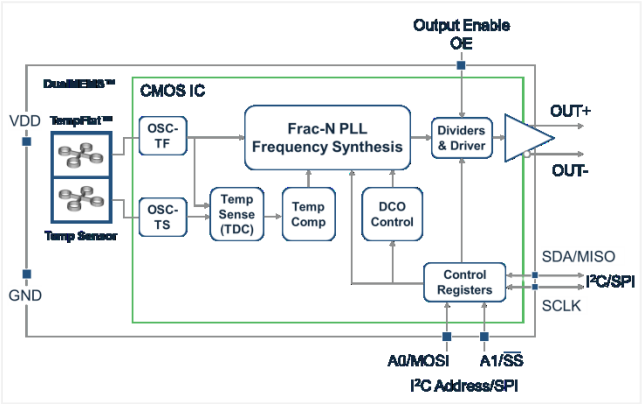


Figure 1. SiT3521 Block Diagram

Package Pinout (10-Lead QFN, 5.0 x 3.2 mm)

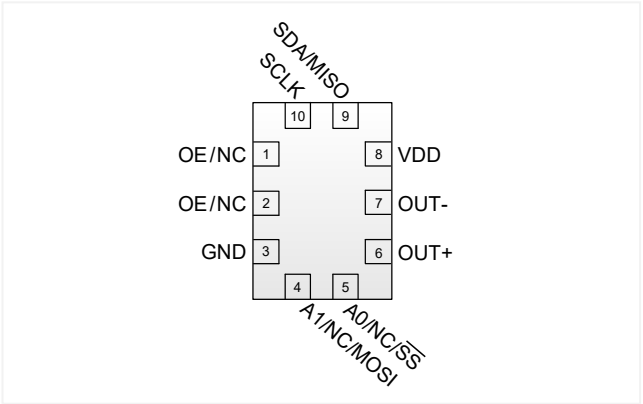


Figure 2. Pin Assignments (Top view)
(Refer to Table 14 for Pin Descriptions)

Ordering Information

SiT3521 AC - 1C 1331 GG 156.250000 T

Part Family
"SiT3521"

Revision Letter
"A" is the revision of Silicon

Temperature Range
"C": Extended Commercial, -20 to 70°C
"I": Industrial, -40 to 85°C
"E": Extended Industrial, -40 to 105°C[1]

Signaling Type
"1": LVPECL
"2": LVDS
"4": HCSL

Package Size
"C": 5.0 x 3.2 mm

Frequency Stability/Grade
"F": ±10 ppm
"1": ±20 ppm
"2": ±25 ppm
"3": ±50 ppm

Voltage Supply
"25": 2.5V ±10%
"28": 2.8V ±10%
"30": 3.0V ±10%
"33": 3.3V ±10%

OE Pin Control
"-": OE under software Control.
Pin 1 and 2 are both NC.
"1": Pin 1 OE, Pin 2 NC
"2": Pin 1 NC, Pin 2 OE

Packaging
"T": 12 mm Tape & Reel, 3ku reel
"Y": 12 mm Tape & Reel, 1ku reel
Leave Blank for Bulk [2]

Frequency
1.000000 to 340.000000 MHz

DCXO Pull Range
"M": ±25 ppm
"B": ±50 ppm
"C": ±80 ppm
"E": ±100 ppm
"F": ±125 ppm
"G": ±150 ppm
"H": ±200 ppm
"X": ±400 ppm
"L": ±600 ppm
"Y": ±800 ppm
"S": ±1200 ppm
"Z": ±1600 ppm
"U": ±3200 ppm

Serial IF mode
"S": SPI mode [1]
"0-G": I²C mode (See below)

I²C Factory Programmable Addresses
"0-F": I²C Address factory programmed
Sets Bits 3:0 of Device I²C address to the Hex value of the ordering code.
When the I²C address is factory programmed using these codes, pin A0, A1 are NC

"G": I²C address controlled by A0, A1 pins

A1:A0	I²C Address
00	1100000
01	1100010
10	1101000
11	1101010 (default)

Notes:
1. -40 to 105°C option available only for I²C operation.
2. Bulk is available for sampling only.

TABLE OF CONTENTS

1 Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output terminations shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Table 1. Electrical Characteristics – Common to LVPECL, LVDS and HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	1	–	340	MHz	Factory or user programmable, accurate to 6 decimal places
Frequency Stability						
Frequency Stability	F_stab	-10	–	+10	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations.
		-20	–	+20	ppm	
		-25	–	+25	ppm	
		-50	–	+50	ppm	
First Year Aging	F_1y	–	±1	–	ppm	1st-year aging at 25°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
		-40	–	+105	°C	Extended Industrial. Available only for I²C operation, not SPI.
Supply Voltage						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.7	3.0	3.3	V	
		2.52	2.8	3.08	V	
		2.25	2.5	2.75	V	
Input Characteristics – OE Pin						
Input Voltage High	VIH	70%	–	–	Vdd	OE pin
Input Voltage Low	VIL	–	–	30%	Vdd	OE pin
Input Pull-up Impedance	Z_in	–	100	–	kΩ	OE pin, logic high or logic low
Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Startup and Output Enable/Disable Timing						
Start-up Time	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value
Output Enable/Disable Time – Hardware control via OE pin	T_oe_hw	–	–	3.8	µs	Measured from the time OE pin reaches rated VIH and VIL to the time clock pins reach 90% of swing and high-Z. See Figure 9 and Figure 10
Output Enable/Disable Time – Software control via I²C/SPI	T_oe_sw	–	–	6.5	µs	Measured from the time the last byte of command is transmitted via I²C/SPI (reg1) to the time clock pins reach 90% of swing and high-Z. See Figure 30 and Figure 31

Table 2. Electrical Characteristics – LVPECL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	89	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	58	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	32	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	Vdd - 1.1V	–	Vdd - 0.7V	V	See Figure 5
Output Low Voltage	VOL	Vdd - 1.9V	–	Vdd - 1.5V	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	225	290	ps	20% to 80%, see Figure 6
Jitter						
RMS Phase Jitter (random) – DCO Mode Only	T_phj	–	0.225	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels
		–	0.1	0.14	ps	f = 156.25, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdd levels
RMS Phase Jitter (random) – Any-frequency Mode Only	T_phj	–	0.225	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels
		–	0.11	0.15	ps	f = 156.25, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdd levels
RMS Period Jitter[3]	T_jitt	–	1	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V

Note:

3. Measured according to JESD65B.

Table 3. Electrical Characteristics – LVDS Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	80	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	61	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Output Characteristics						
Differential Output Voltage	VOD	250	–	455	mV	f = 156.25MHz See Figure 7
Delta VOD	ΔVOD	–	–	50	mV	See Figure 7
Offset Voltage	VOS	1.125	–	1.375	V	See Figure 7
Delta VOS	ΔVOS	–	–	50	mV	See Figure 7
Rise/Fall Time	Tr, Tf	–	400	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 8
Jitter						
RMS Phase Jitter (random) – DCO Mode Only	T_phj	–	0.21	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels
		–	0.1	0.12	ps	f = 156.25, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdd levels
RMS Phase Jitter (random) – Any-frequency Mode Only	T_phj	–	0.21	0.367	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels
		–	0.1	0.12	ps	f = 156.25, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdd levels
RMS Period Jitter[4]	T_jitt	–	1	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V

Note:

4. Measured according to JESD65B.

Table 4. Electrical Characteristics – HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	93	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	60	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	35	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	0.60	–	0.90	V	See Figure 5
Output Low Voltage	VOL	-0.05	–	0.08	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1.2	1.4	1.8	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	360	465	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 6
Jitter						
RMS Phase Jitter (random) – DCO mode only	T_phj	–	0.215	0.280	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz all Vdd levels
		–	0.09	0.12	ps	f = 156.25 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdd levels
RMS Phase Jitter (random) – Any-frequency mode only	T_phj	–	0.220	0.320	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels
		–	0.1	0.12	ps	f = 156.25 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdd levels
RMS Period Jitter[5]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V

Note:

5. Measured according to JESD65B.

Table 5. I²C Electrical Characteristics – SCLK, SDA, 1 MHz SCLK, 255 Ohm, 550 pF (Max I²C Bus Load)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Voltage Low	VIL	–	–	30%	Vdd	
Input Voltage High	VIH	70%	–	–	Vdd	
Output Voltage Low	VOL	–	–	0.4	V	
Input Leakage current[6]	I_L	0.5	–	24	µA	0.1 Vdd < VOUT < 0.9 Vdd
Input Capacitance	C_{IN}	–	–	5	pF	

Note:

6. Including leakage current from 160 kOhm pull resister at typical condition to Vdd.

Table 6. SPI Electrical Characteristics – SCLK, MOSI, $\overline{SS}$, MISO

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Pins – SCKL, MOSI, $\overline{SS}$						
Input Voltage Low	VIL	–	–	10%	Vdd	
Input Voltage High	VIH	90%	–	–	Vdd	
Input Capacitance	C_{IN}	–	–	5	pF	
Output Pin – MISO						
Output Voltage High	VOH	90%	–	–	Vdd	IOH = 2.2 mA (Vdd = 2.5V)
Output Voltage Low	VOL	–	–	10%	Vdd	IOL = 2.7 mA (Vdd = 2.5V)
Leakage in high impedance mode	I_L	0.5	–	24	µA	0.1 Vdd< VOUT < 0.9 Vdd

Table 7. Typical Phase Noise: Default start-up or reprogrammed frequency in DCO mode – LVDS output clock

Frequency Offsets	Output Frequency Phase Noise (dBc/Hz)	
	156.25 MHz	322.265625 MHz
100 Hz	-97.8	-91.5
1 kHz	-122.9	-116.5
10 kHz	-131.1	-124.6
100 kHz	-132.9	-126.3
1 MHz	-148.2	-132.0
10 MHz	-156.9	-153.0
20 MHz	-157.7	-154.2

Table 8. Typical Phase Noise: Reprogrammed frequency in any-frequency Mode – LVDS output clock

Frequency Offsets	Output Frequency Phase Noise (dBc/Hz)	
	156.25 MHz	322.265625 MHz
100 Hz	-98.5	-92.7
1 kHz	-123.0	-116.6
10 kHz	-131.9	-125.3
100 kHz	-134.8	-127.9
1 MHz	-146.9	-131.2
10 MHz	-156.7	-152.7
20 MHz	-157.7	-154.1

Table 9. Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Vdd	-0.5	4.0	V
VIH	–	Vdd + 0.3V	V
VIL	-0.3	–	V
Storage Temperature	-65	150	ºC
Maximum Junction Temperature	–	130	ºC
Soldering Temperature[7] (follow standard Pb-free soldering guidelines)	–	260	ºC

Note:

7. Exceeding this temperature for an extended period of time may damage the device.

Table 10. Thermal Consideration[8]

Package	θJA, 4 Layer Board (°C/W)	θJC, Bottom (°C/W)
5032, 10-pin	55	20

Note:

8. Refer to JESD51 for θJA and θJC definitions, and reference layout used to determine the θJA and θJC values in the above table.

Table 11. Maximum Operating Junction Temperature[9]

Max Operating Temperature(ambient)	Maximum Operating Junction Temperature
70°C	95°C
85°C	110°C
105°C	130°C

Note:

9. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 12. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	*G*
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	*G*
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C	–	–
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

2 Device Configurations and Pin-outs

Table 13. Device Configurations

Programming Interface	Addressing Mode	Pin 4	Pin 5	Pin 9	Pin 10
I²C	Pin controlled	A1	A0	SDA	SCLK
	Software	NC	NC	SDA	SCLK
SPI	–	$\overline{SS}$	MOSI	MISO	SCLK

Pin-out Top Views (10-Lead QFN, 5.0 mm x 3.2 mm)

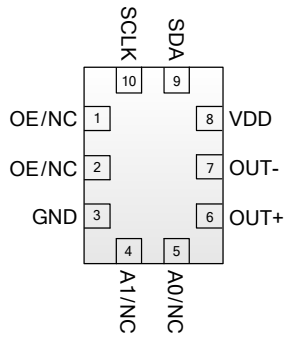


Figure 3. I²C Mode

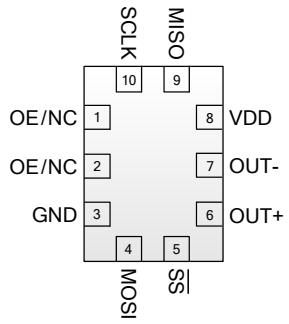


Figure 4. SPI Mode

Table 14. Pin Description

Pin	Symbol	I/O	Internal Pull-up/ Pull Down Resistor	Function
1	OE	Input	100 kΩ Pull-Up	Pin 1 and Pin 2 functions are set by the ordering code in Ordering Information Table. If Software OE mode is selected in Ordering Table, both pin 1 and pin 2 are NC. H[10]: Specified frequency output L: Output Driver is disabled: OUT- = High-Z OUT+ = High-Z
	NC	No Connect		No Connect
2	OE	Input	100 kΩ Pull-Up	Pin 1 and Pin 2 functions are set by the ordering code in Ordering Information Table. If Software OE mode is selected in Ordering Table, both pin 1 and pin 2 are NC. H[10]: Specified frequency output L: Output Driver is disabled: OUT- = High-Z OUT+ = High-Z
	NC	No Connect		No Connect
3	GND	Ground		Connect to ground
4	A1	Input	100 kΩ Pull-Up	I²C Address Select, Most Significant Bit (MSB) A1 A0 I²C Address 0 0 1100000 0 1 1100010 1 0 1101000 1 1 1101010 (Default)
	NC	No Connect		No Connect. I²C Address is factory set to one of the 16 available addresses shown in Table 27 and also on the Ordering Information Table.
	$\overline{SS}$	Input	100 kΩ Pull-Up	SPI Chip select, active low
5	A0	Input	100 kΩ Pull-Up	I²C Address Select, Least Significant Bit (LSB) A1 A0 I²C Address 0 0 1100000 0 1 1100010 1 0 1101000 1 1 1101010 (Default)
	NC	No Connect		No Connect. I²C Address is factory set to one of the 16 available addresses shown in Table 27 and also on the Ordering Information Table.
	MOSI	Input	100 kΩ Pull-Up	SPI serial data input
6	OUT+	Output		Oscillator output
7	OUT-	Output		Complementary oscillator output
8	VDD	Power		Connect to Vdd[11]
9	SDA	Input	200 kΩ Pull-Up	I²C serial data input
	MISO	Output	200 kΩ Pull-Up	SPI serial data output
10	SCLK	Input	200 kΩ Pull-Up	I²C/SPI serial clock input

Notes:

10. In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If OE pin needs to be left floating, use the NC option.
11. 0.1 µF capacitor in parallel with a 10 µF capacitor are required between VDD and GND.

3 Waveform Diagrams

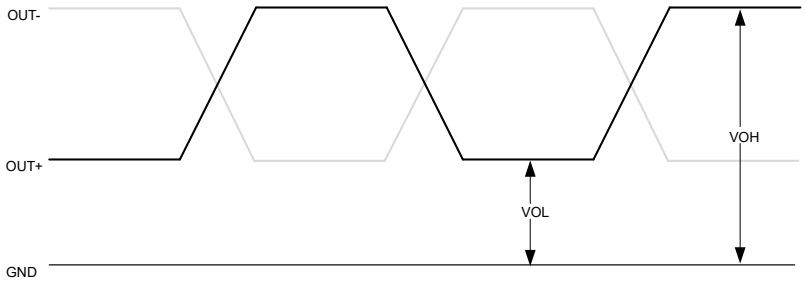


Figure 5. LVPECL, HCSL Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)

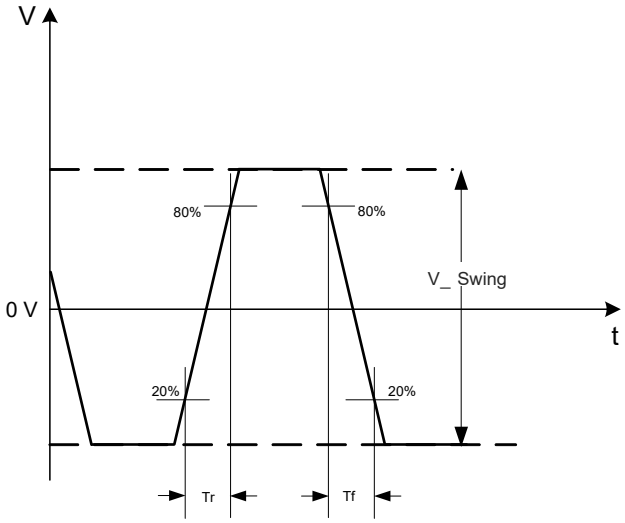


Figure 6. LVPECL, HCSL Voltage Levels Across Differential Pair (i.e. OUT+ minus OUT-)

Waveform Diagrams (continued)

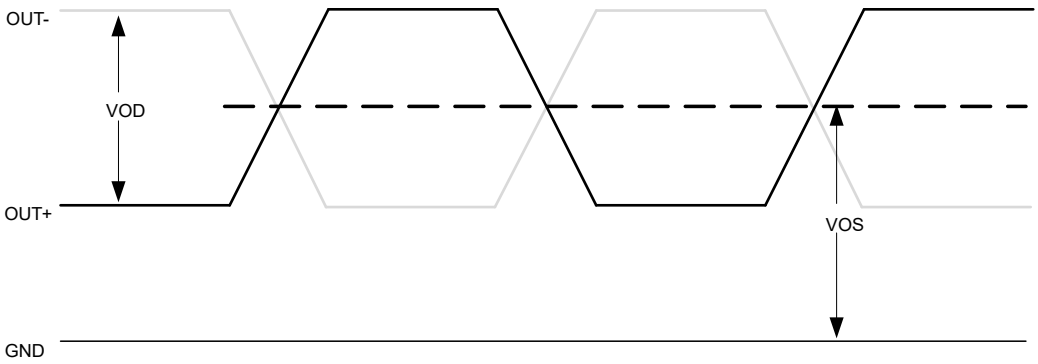


Figure 7. LVDS Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)

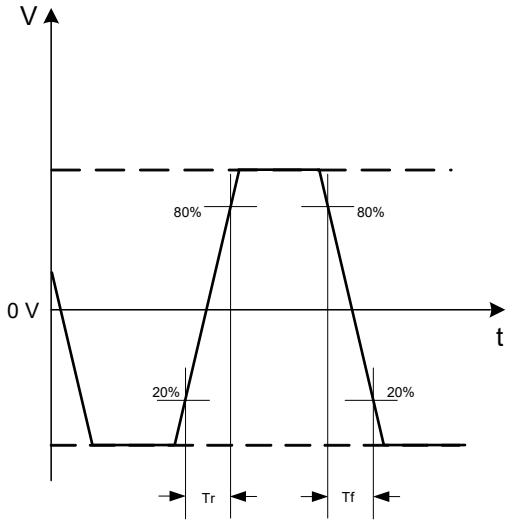


Figure 8. LVDS Differential Waveform (i.e. OUT+ minus OUT-)

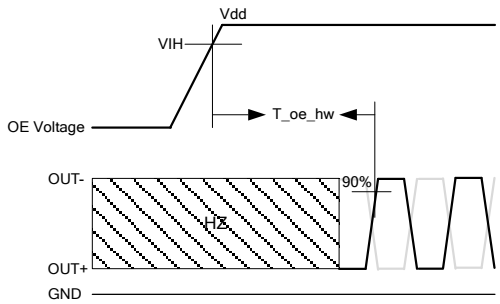


Figure 9. Hardware OE Enable Timing

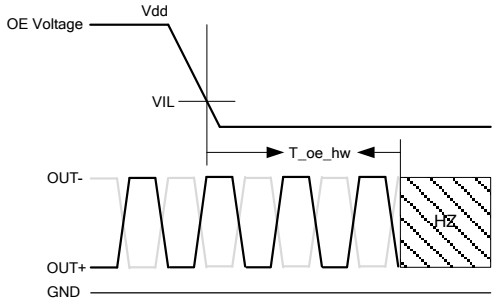


Figure 10. Hardware OE Disable Timing

4 Termination Diagrams

4.1. LVPECL

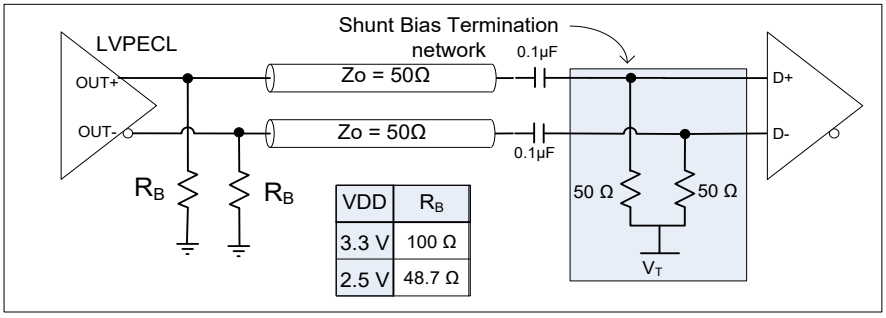


Figure 11. LVPECL with AC-coupled Termination

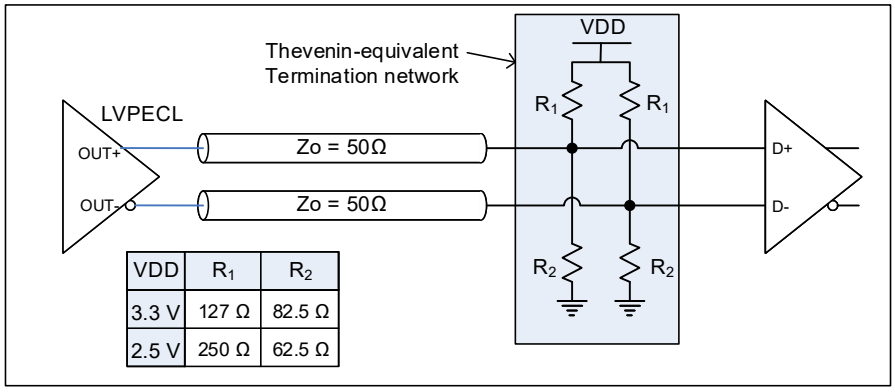


Figure 12. LVPECL DC-coupled Load Termination with Thevenin Equivalent Network

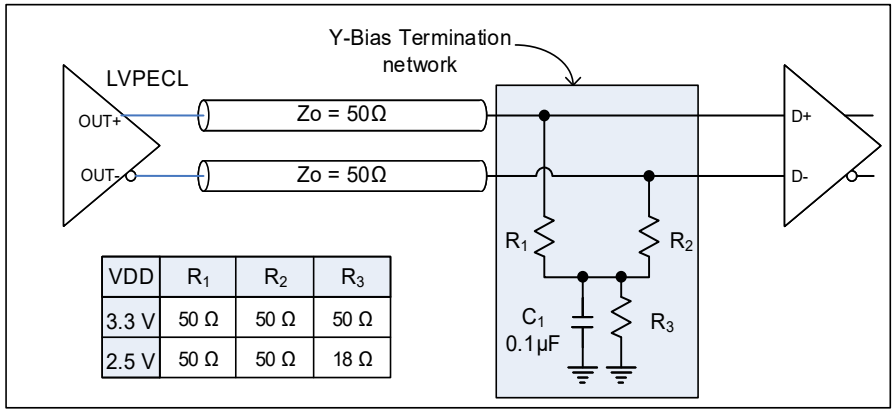


Figure 13. LVPECL with Y-Bias Termination

Termination Diagrams (continued)

LVPECL (continued)

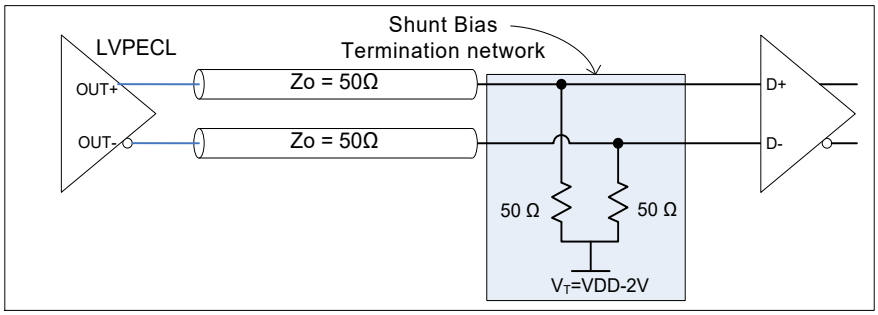


Figure 14. LVPECL with DC-coupled Parallel Shunt Load Termination

Termination Diagrams (continued)

4.2. LVDS

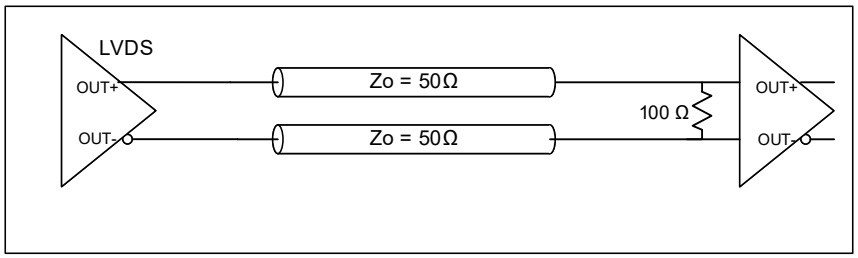


Figure 15. LVDS single DC Termination at the Load

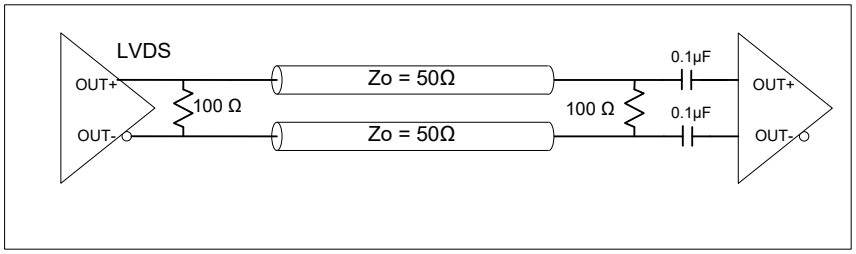


Figure 16. LVDS Double AC Termination with Capacitor Close to the Load

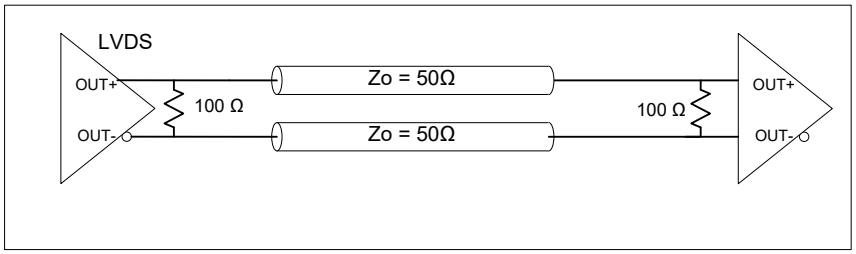


Figure 17. LVDS Double DC Termination

Termination Diagrams (continued)

4.3. HCSL

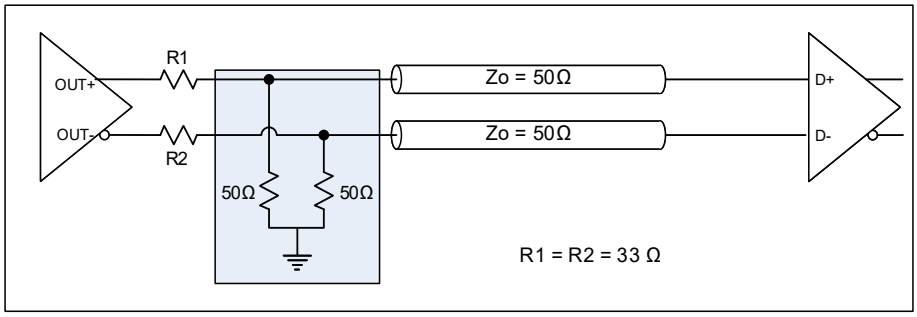


Figure 18. HCSL Interface Termination

5 Test Circuit Diagrams

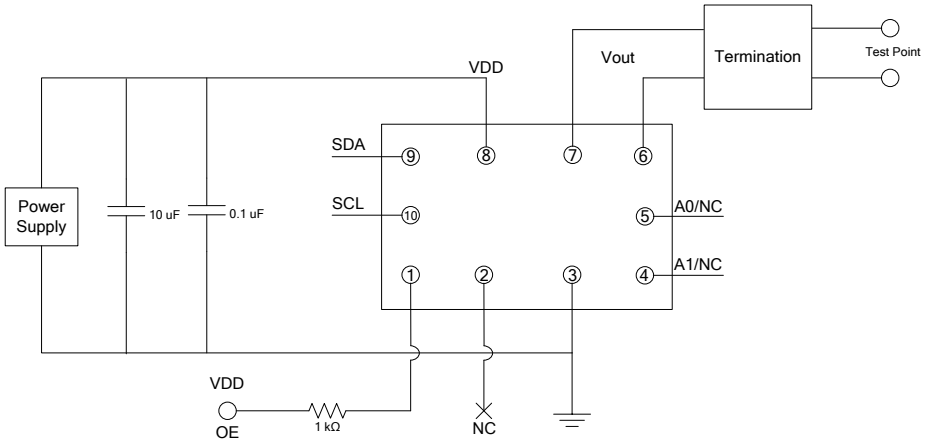


Figure 19. Test Circuit (I²C mode and OE Function for Pin 1)

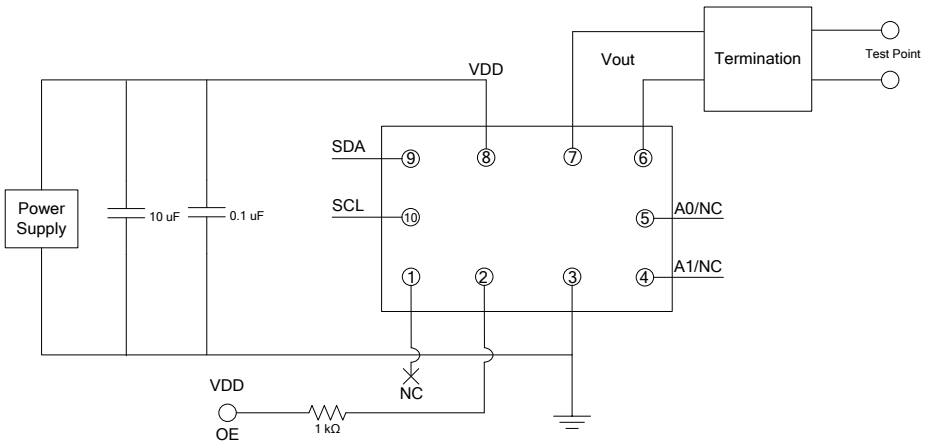


Figure 20. Test Circuit (I²C mode and OE Function for Pin 2)

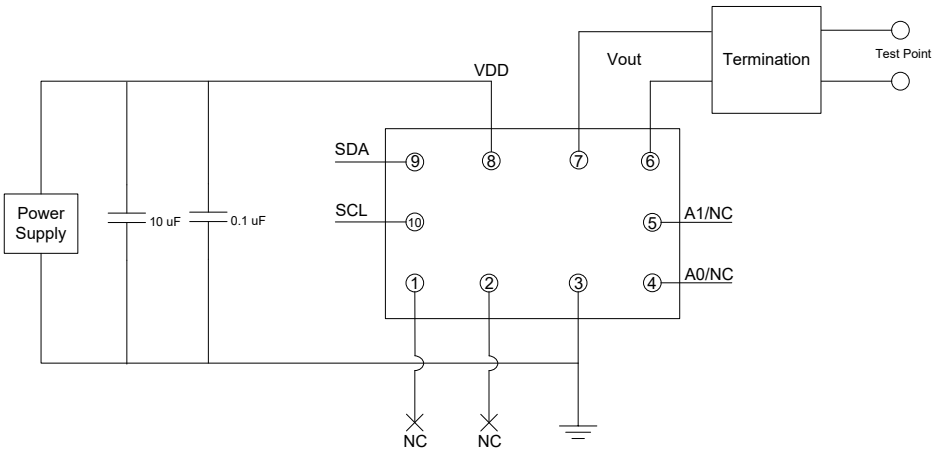


Figure 21. Test Circuit (I²C mode and NC Function for both Pin1 and Pin2)

Test Circuit Diagrams (continued)

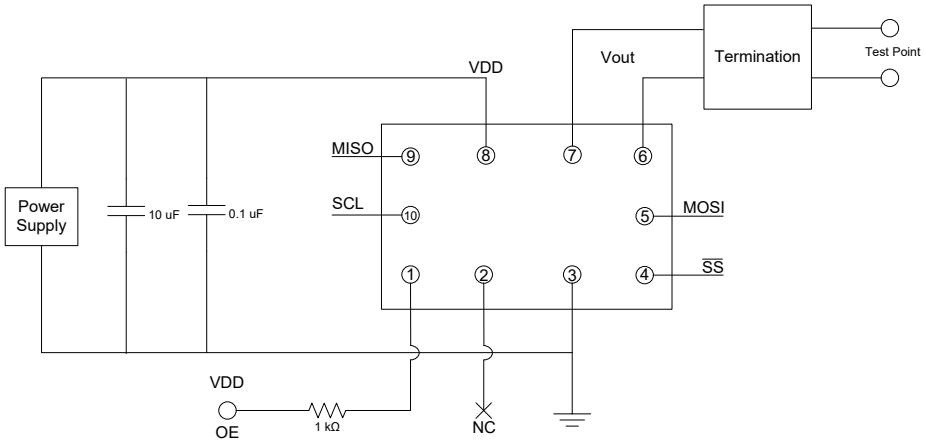


Figure 22. Test Circuit (SPI mode and OE Function for Pin 1)

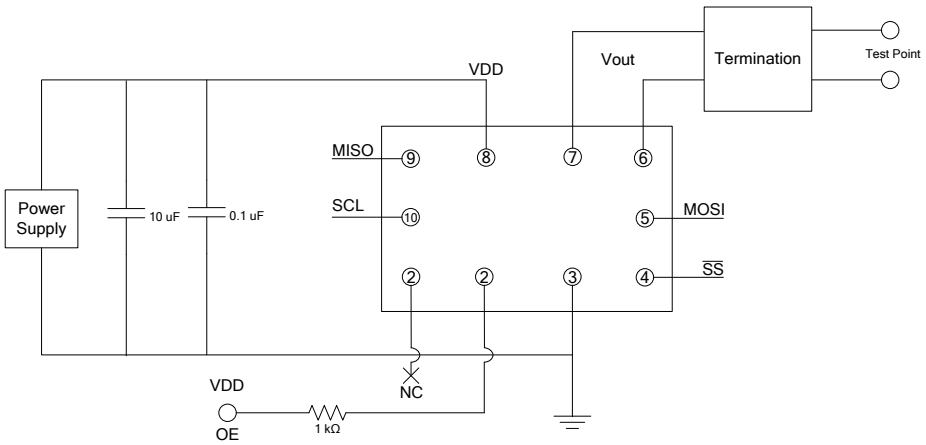


Figure 23. Test Circuit (SPI mode and OE Function for Pin 2)

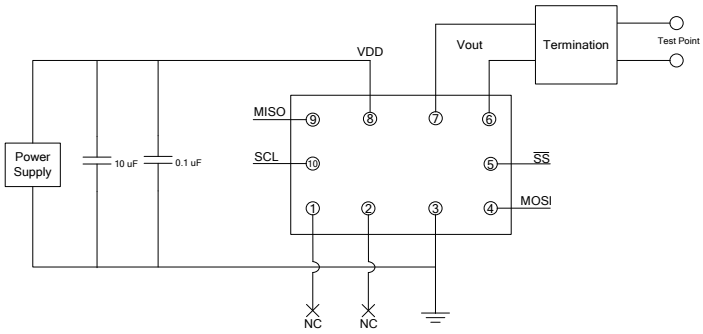


Figure 24. Test Circuit (SPI mode and NC Function for both Pin1 and Pin2)

6 Architecture Overview

Based on SiTime's innovative Elite Platform™, the SiT3521 delivers exceptional dynamic performance, i.e. resilience to environmental stressors such as shock, vibration and fast temperature transients. Underpinning the Elite platform are SiTime's unique DualMEMS™ temperature sensing architecture and TurboCompensation™ technology, illustrated in Figure 1.

DualMEMS is a noiseless temperature sensing scheme. It consists of two MEMS resonators fabricated on the same die substrate. The TempFlat resonator is designed with a flat frequency characteristic over temperature whereas the temperature sensing resonator is by design sensitive to temperature changes. The ratio of frequencies between these two resonators provides an accurate reading of the resonator temperature with 30 µK resolution.

By placing the two MEMS resonators on the same die, this temperature sensing scheme eliminates the thermal lag and gradients between the resonator and the temperature sensor, an inherent weakness of the legacy quartz TCXOs.

The DualMEMS temperature sensor is then combined with a state-of-the-art temperature compensation circuit in the CMOS IC. The TurboCompensation design, with >100 Hz compensation bandwidth, achieves dynamic frequency stability that is far superior to any quartz devices. The 7th order compensation algorithm enables additional optimization of frequency stability and frequency slope over temperature within any specific temperature range of choice for a given system design.

The Elite platform also incorporates a high resolution, low noise frequency synthesizer along with the industry standard I²C and/or SPI bus. This unique combination enables system designers to digitally control the output frequency in steps as low as 5 ppt (parts per trillion) and over a wide frequency range from 1 MHz to 340 MHz.

For more information regarding the Elite platform and its benefits please visit:

- SiTime's breakthroughs section
- TechPaper: DualMEMS Temperature Sensing Technology
- TechPaper: DualMEMS Resonator TDC

7 Functional Overview

The SiT3521 is designed for maximum frequency flexibility with an array of factory programmable options, enabling system designers to configure this precision device for optimal performance in a given application.

7.1. User Programming Interface

The SiT3521 supports either I²C or SPI interface (slave only) as a factory programmable option via the ordering codes For I²C, the user has the option of using one of the four default addresses selectable with two address pins (A0, A1) or specifying one of the sixteen factory programmed addresses. Refer to I²C/SPI Device Address Modes section for details.

Table 15. Programming Interface Ordering Codes

Programming Interface	Addressing Mode	Ordering Code
I²C	2 address pins – A0, A1	"G"
	Factory programmed	"0-F"
SPI	Chip select pin	"S"

7.2. Start-up output frequency and signaling types

The SiT3521 is shipped with a default start-up frequency between 1 MHz to 340 MHz in steps of 1 Hz that a user specifies in the ordering code.

A user can also specify one of the three differential signaling types in the ordering code.

Table 16. Output Format Ordering Codes

Output Format	Ordering Code
LVPECL	"1"
LVDS	"2"
HCSL	"4"

7.3. In-system programmable options

The SiT3521 enables software control of the following features via I²C/SPI:

- **Any-frequency feature**: Output frequency that can be re-programmed to any value between 1 MHz and 340 MHz in 1 Hz steps
- **DCO feature**: Output frequency that can be steered (pulled) by up to ±3200 ppm with 5 to 94 ppt resolution
- **Software OE feature**: Enabling or disabling of the output driver

Refer to Chapter 9 for programming details.

8 In-system Programmable Functional Description

Figure 25 shows hi-level block diagram of In-system programmable oscillator showing user accessible and non-user-accessible circuit blocks.

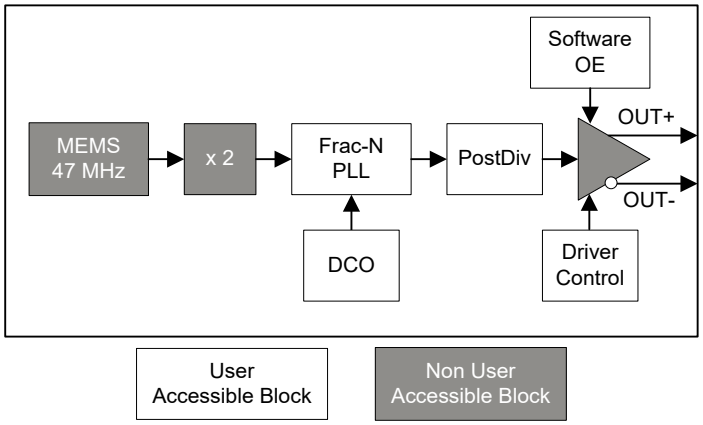


Figure 25. In-system Programmable Oscillator Block Diagram

8.1. Any-frequency function

The any-frequency feature allows users to re-program the device output to a new frequency between 1 MHz to 340 MHz and optimize output driver according to the given new frequency after power-up through the I²C or SPI interface. Device output frequency is defined by a combination of Frac-N PLL and post-divider.

Equation 1: Output frequency,

$$Fout = \frac{47\ MHz * Frac\text{-}N\ PLL * 2}{postDiv}$$

Table 17 is showing unsupported any-frequency Frequencies.

Table 17. List of Unsupported Frequencies

Unsupported Frequency Range (MHz)	
Min.	Max.
300.600000	307.499000

To re-program device to the desired output frequency, user should calculate the most appropriate Frac-N PLL and post divider combination. For a given output frequency, the choice of dividers combination must fall within the allowable ranges (See the Table 18).

Calculation of the appropriate Frac-N PLL and postDiv values and selection of proper Driver Control values consist of the following steps. Throughout these steps, and example using LVPECL 75 MHz output frequency will be used.

Table 18. Any-frequency user-accessible blocks

Block Name	Available values	Register Name	Register Address
Frac-N PLL	13.08511 to 15.96875	Frac-N PLL [31:0]	0x03[15:0] = Frac-N PLL[31:16] 0x04[15:0] = Frac-N PLL[15:0]
PostDiv	2 to 8191	PostDiv [12:0]	0x05[15:3] = PostDiv[12:0]
Driver Control	0 to 63	Driver Control [5:0]	0x05[2:0] = Driver Control [5:3] 0x06[2:0] = Driver Control [2:0]

Step 1: Frac-N PLL and PostDiv value calculation

Find the lowest allowed postDiv value which gives Frac-N PLL value (see Equation 2) within allowed Frac-N PLL range (see Table 18):

Equation 2:

$$Frac\text{-}N = \frac{Fout * postDiv}{47MHz * 2} = \frac{Fout * postDiv}{94\ MHz}$$

Table 19 below shows implementation of this step for the 75 MHz output frequency example. The combination satisfying above conditions is highlighted in **blue**.

Table 19. Frac-N PLL and postDiv Combination Calculation for Output Frequency = 75 MHz

PostDiv Within 2 to 8191	Frac-N PLL Within 13.08511 to 15.96875
16	12.76596
17	13.56383
18	14.36170
19	15.15957
20	15.95745

Step 2: Calculate Frac-N PLL and postDiv Binary Values

The selected combination of Frac-N PLL and postDiv values should be converted to binary words and then written to the device's control registers. Number conversion, conditioning and write procedure are as follows. The values calculated in the previous steps for 75 MHz output frequency will be used for example purposes.

Step 2.1: Convert Frac-N PLL value to binary word

32 bits are intended for Frac-N PLL value: MSB 5 bits for integer and LSB 27 for fractional parts

1) Take the integer part of the Frac-N PLL value and convert to binary.
   In our example, integer part is Dec:13 and bin:01101
2) Execute bitwise XOR operation on the integer part (01101b) and 01110b mask.
   The reason for the 01110b mask is to set the default value when the device is in an un-programmed state and all bit values are 0.

Frac-N PLL[31:27] = 01101b (given integer part)
XOR 01110b (mask) = 00011b (final value)

3) Fractional part of the Frac-N PLL value should be multiplied by 2^{27} and then rounded towards nearest integer. Then it should be converted to binary value resulting in a 27-bit binary word. Because the fractional part of Frac-N PLL is always positive, no sign bit should be used. In our example,
   2^{27} * 0.85869 = 115,251,420.856. Rounding to the nearest integer gives 115,251,421 and converting
   to binary:

Frac-N PLL[26:0] =
11011011110100110001101110 1b (final value)

Step 2.2: Convert postDiv value to binary word

1) PostDiv value should be converted to 13-bit binary word. As post divider is always positive no sign bit should be used.
   In this example, the PostDiv value is Dec:17, bin: 0000000010001b
2) Execute bitwise XOR operation on the PostDiv value and 0000000011011b mask.

PostDiv[12:0] = 0000000010001b (given postDiv)
XOR 0000000011011b = 0000000001010b (final value)

Step 3: Select appropriate Drive Control values

Select appropriate Drive Control values based on Table 20.

Table 20. Driver Control settings

Output Driver	Output Frequency (MHz)	Drive Control [5:0]
LVPECL	1 to 250	110110b
	250.000001 to 340	101110b
LVDS or HCSL	1 to 250	001000b
	250.000001 to 340	000000b

In the example, **Drive Control[5:0]: = 110110b**

Step 4: Write Frac-N PLL and PostDiv binary values to the device

Step 4.1: Read back the contents of 0x06[15:0]

Reg6 read back is needed to capture the value of this register so the same values can be written along with the Driver Control[2:0] value

Step 4.2: Write registers to the device in the following sequence

1) Address 0x03
0x03[15:11] = Frac-N PLL[31:27] (integar part)
0x03[10:0] = Frac-N PLL[26:16] (fractional part, MSB)
2) Address 0x04
0x04[15:0] = FFrac-N PLL[15:0] (fractional part, LSB)
3) Address 0x06
0x06[15:3] = Values red out at step 3.1
0x06[2:0] = Driver Control[2:0]
4) Address 0x05
0x05[15:3] = PostDiv[12:0]
0x05[2:0] = Driver Control[5:3]

After the post-divider value 0x05 is written, the outputs will be disabled until the PLL locks to the new frequency and is stable. When the PLL is stable, the clock output will be re-enabled. Figure 26 and Figure 27 show the write sequence, output disable and programming time for I²C and SPI interfaces.

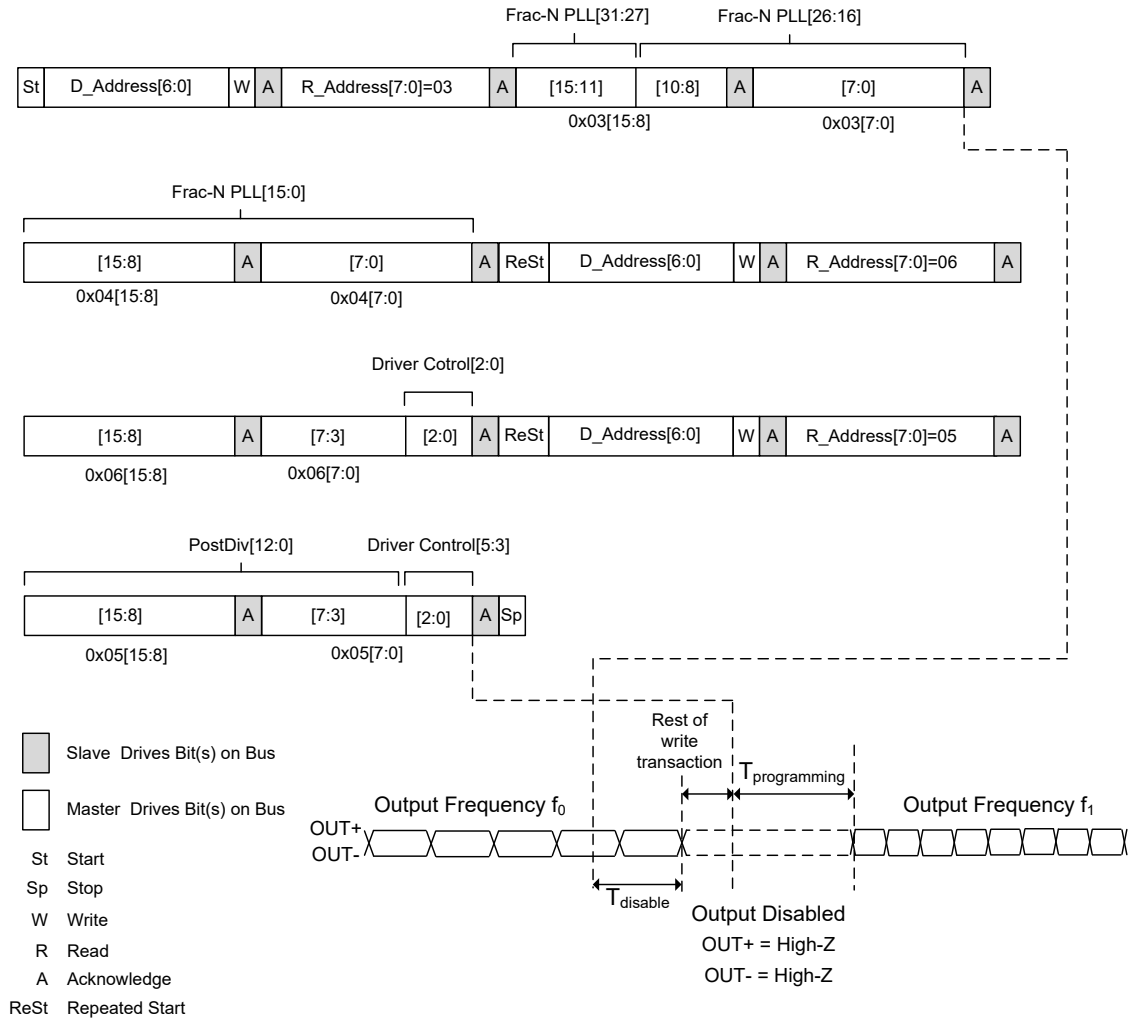


Figure 26. Changing the Default Start-up Output Frequency Using Auto Address Incrementing (I²C)

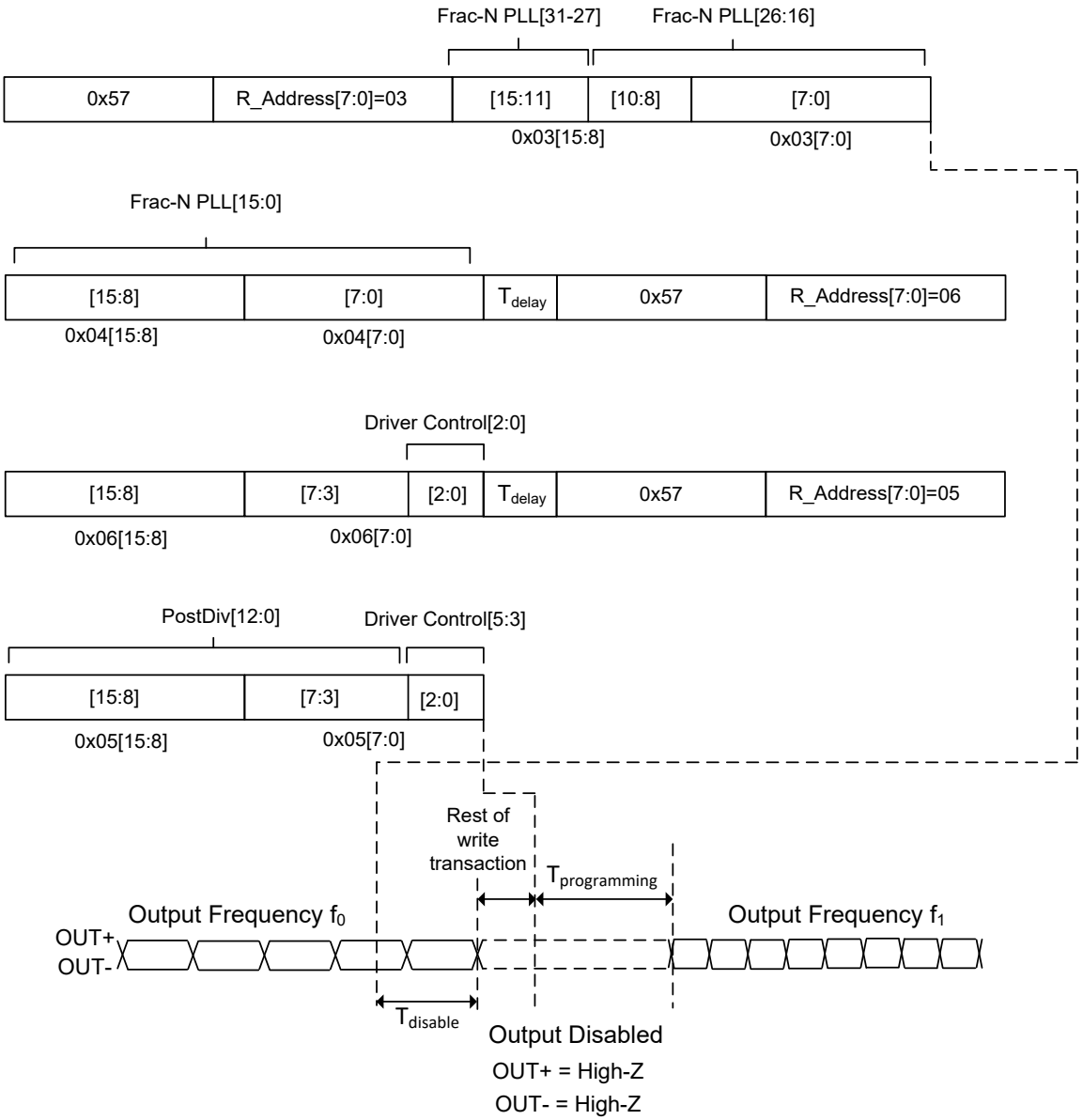


Figure 27. Changing the Default Start-up Output Frequency Using Auto Address Incrementing (SPI)

Table 21. Output Disable and Enable Times when Changing the output frequency

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Delay between transactions	T_{delay}	125	–	–	µs	SPI only
Output Disable Time	$T_{disable}$	–		2.3	µs	
Re-programming Time	$T_{re\text{-}programming}$	–		421	µs	

8.2. DCO Functional Description

The DCO feature allows users to steer (pull) output frequency by up to ±3200 ppm with 5 to 94 ppt resolution through the I²C or SPI digital interface.

There are several advantages of DCO relative to analog voltage control (VCXO)

a. Frequency Control Resolution as low as 5 ppt. This high resolution minimizes accumulated time error in synchronization applications.
b. Lower system cost – A VCXO may need a Digital to Analog Converter (DAC) to drive the control voltage input. In a DCO, the frequency control is achieved digitally by register writes to the control registers via I²C, thereby eliminating the need for a DAC.
c. Better Noise Immunity – The analog signal used to drive the voltage control pin of a VCXO can be sensitive to noise and the trace over which the signal is routed can be susceptible to noise coupling from the system. The DCO does not suffer from analog noise coupling since the frequency control is performed digitally through I²C.
d. No Frequency Pull non-linearity. The frequency pulling is achieved via fractional feedback divider of the PLL, eliminating any pull non-linearity concern which is typical of quartz based VCXOs. This improves dynamic performance in closed loop operations.
e. Programmable Wide Pull Range – The DCO pulling mechanism is via the fractional feedback divider and is therefore not constrained by resonator pullability as in quartz based solutions. The SiT3521 offers 16 frequency pull range options from ±6.25 ppm to ±3200 ppm, thereby giving system designers great flexibility.

In the DCO mode, the device powers up at the nominal operating frequency and pull range specified by the ordering code. After power-up both the pull range and output frequency can be controlled via I²C/SPI writes to the respective control registers. The maximum output frequency change is constrained by the pull range limits.

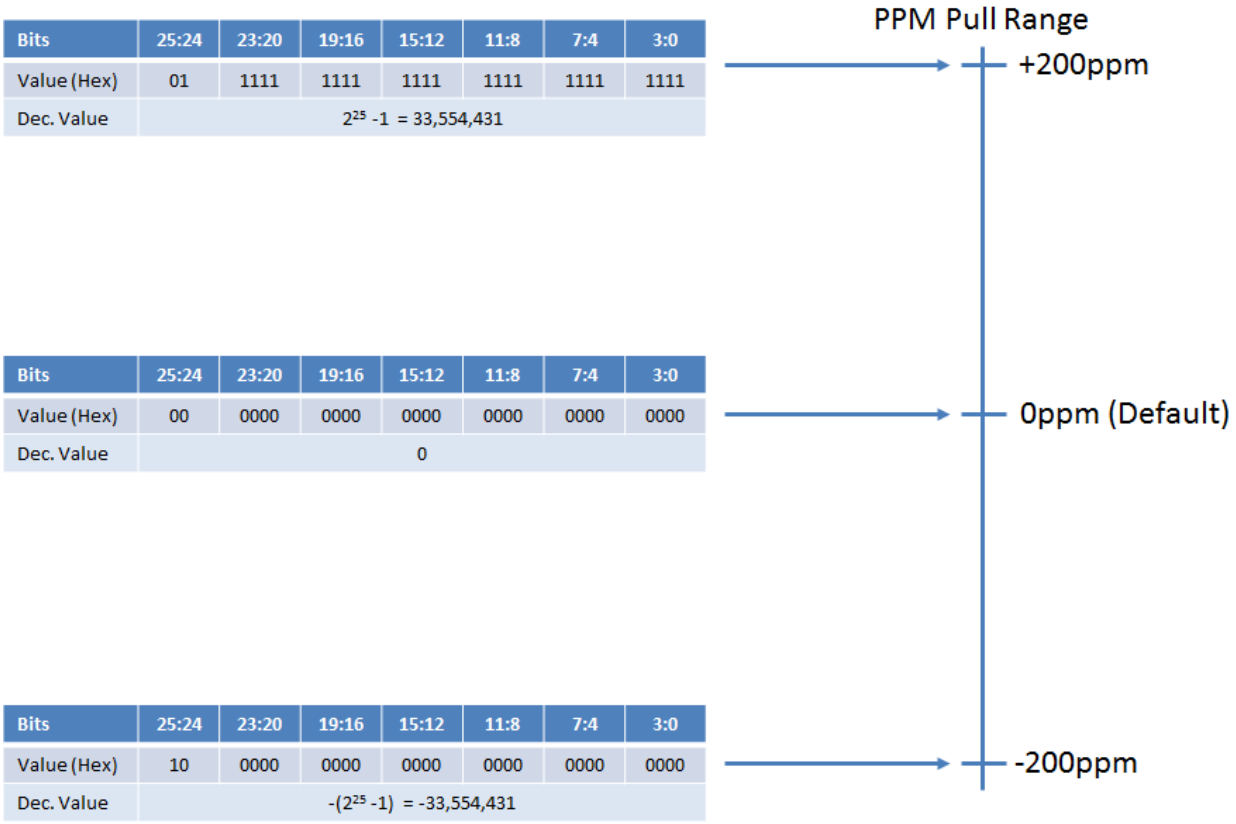
The pull range is specified by the value loaded in the digital pull range control register. The 16 pull range choices are specified in the control register and range from ±6.25 ppm to ±3200 ppm.

Table 22 below shows the frequency resolution vs. pull range programmed value.

Table 22. Frequency Resolution vs. Pull Range

Programmed Pull Range	Frequency Precision
±25 ppm	$5x10^{-12}$
±50 ppm	$5x10^{-12}$
±80 ppm	$5x10^{-12}$
±100 ppm	$5x10^{-12}$
±125 ppm	$5x10^{-12}$
±150 ppm	$5x10^{-12}$
±200 ppm	$5x10^{-12}$
±400 ppm	$1x10^{-11}$
±600 ppm	$1.4x10^{-11}$
±800 ppm	$2.1x10^{-11}$
±1200 ppm	$3.2x10^{-11}$
±1600 ppm	$4.7x10^{-11}$
±3200 ppm	$9.4x10^{-11}$

The ppm frequency offset is specified by the 26-bit DCO Frequency control register in two's complement format as described in the I²C/SPI Register Descriptions. The power up default value is 00000000000000000000000000b which sets the output frequency at its nominal value (0 ppm). To change the output frequency, a frequency control word is written to 0x00[15:0] (Least Significant Word) and 0x01[9:0] (Most Significant Word). The LSW value should be written first followed by the MSW value; the frequency change is initiated after the MSW value is written.



Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	01	1111	1111	1111	1111	1111	1111
Dec. Value	2^{25} -1 = 33,554,431						

Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	00	0000	0000	0000	0000	0000	0000
Dec. Value	0						

Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	10	0000	0000	0000	0000	0000	0000
Dec. Value	-(2^{25} -1) = -33,554,431						

Figure 28. Pull range and Frequency Control Word

Figure 28 shows how the two's complement signed value of the frequency control word sets the output frequency within the ppm pull range set by 0x02[3:0]. This example shows use of ±200 ppm pull range. Therefore, to set the desired output frequency, one just needs to calculate the fraction of full scale value ppm, covert to two's complement binary and then write the values to the frequency control registers.

The following formula generates the control word value:

Control word Value =
= RND((2^{25}-1) * ppm shift from nominal/pull range)

where RND is the rounding function which rounds the number to the nearest whole number.

Two examples follow, assuming the ±200 ppm pull range.

Example 1:

Default start-up output frequency = 156.25 MHz
Desired output frequency = 156.2640625 MHz (+90 ppm)

2^{25}-1 corresponds to +200 ppm, and the fractional value required for +90 ppm can be calculated as follows.
90 ppm/200 ppm * (2^{25}-1) = 15,099,493.95

Rounding to the nearest whole number yields 15,099,494 and converting to two complement gives a binary value of 111001100110011001100110 and E66666 in hex.

Example 2:

Default start-up output frequency = 122.88 MHz
Desired output frequency = 122.873856 MHz (-50 ppm)

Following formula shown above,

(-50 ppm/200 ppm) * (225-1) = -8,388,607.75

Rounding to the nearest whole number results in -8,388,608.

Converting to two's complement binary results in 111000000000000000000000000 and 3800000 in hex.

To Summarize, the procedure for calculating the frequency control word associated with a given ppm offset is as follows:

1) Calculate the fraction of the half pull range needed. For example, if the total pull range is set for ±100 ppm and a +20 ppm shift from the nominal frequency is needed, this fraction is 20 ppm/100 ppm = 0.2
2) Multiply this fraction by the full half scale word value, 2^{25}-1 = 33,554,431, round to the nearest whole number and convert the result to two's complement binary. Following the +20 ppm example, this value is 0.2 * 33,554,431 = 6,710,886.2 and rounded to 6,710,886.
3) Write the two's complement binary value starting with the Least Significant Word (LSW) 0x00[16:0], followed by the Most Significant Word (MSW), 0x01[9:0]. If the user desires that the output remains enabled while changing the frequency, a 1 must also be written to the OE control bit 0x01[10] if the device has software OE Control Enabled.

It is important to note that the maximum DCO Frequency Control update rate is 38 kHz regardless of I²C/SPI bus speed.

8.3. Pull Range, Absolute Pull Range

Pull range (PR) is the amount of frequency deviation that will result from changing the control voltage over its maximum range under nominal conditions.

Absolute pull range (APR) is the guaranteed controllable frequency range over all environmental and aging conditions. Effectively, it is the amount of pull range remaining after taking into account frequency stability tolerances over variables such as temperature, power supply voltage, and aging, i.e.:

$$APR = PR - F_{stability} - F_{aging}$$

where $F_{stability}$ is the device frequency stability due to initial tolerance and variations on temperature, power supply, and load.

Table 23 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

Table 23. DCO Pull Range, APR Options

Pull Range Ordering Code	Programmed Pull Range ppm	APR ppm ±10 ppm option	APR ppm ±20 ppm option	APR ppm ±25 ppm option	APR ppm ±50 ppm option
M	±25	±10	–	–	–
B	±50	±35	±25	±20	–
C	±80	±65	±55	±50	±25
E	±100	±85	±75	±70	±45
G	±125	±110	±100	±95	±70
H	±200	±185	±175	±170	±145
X	±400	±385	±385	±380	±345
Y	±800	±785	±785	±780	±745
Z	±1600	±1585	±1585	±1580	±1545
U	±3200	±3185	±3185	±3180	±3145

Figure 29 below shows the I²C sequence for writing the 4-byte control word using auto address incrementing. It is important to note that if the I²C function is under software control, the software OE control bit 0x01[10] should be "1" during the write sequence to avoid disabling the output.

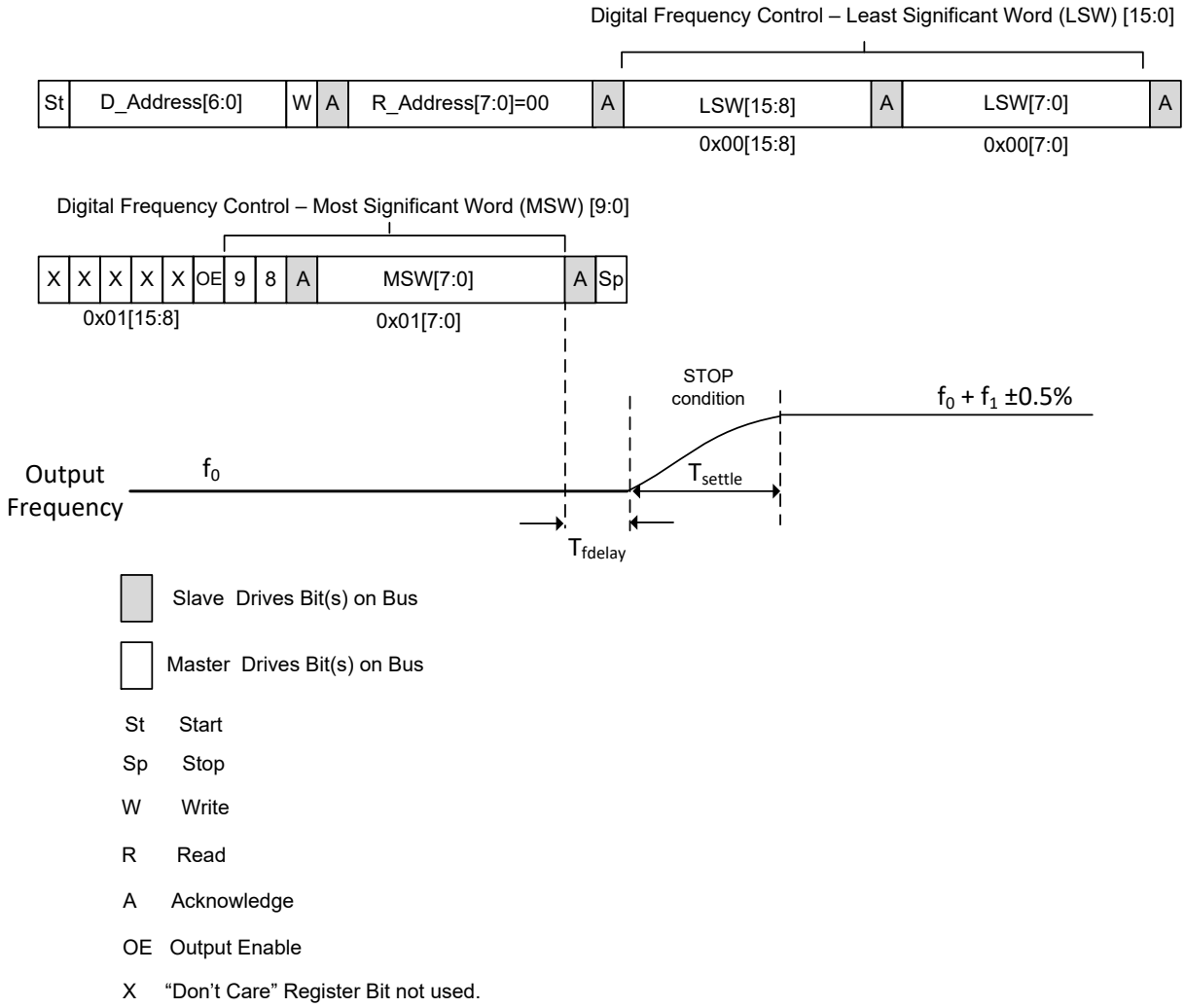


Figure 29. Writing the Frequency Control Word

Table 24. DCO Delay and Settling Time

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Change Delay	T_{fdelay}	–	103	140	µs	Time from end of 0x01 reg MSW to start of frequency pull, as shown in Figure 29
Frequency Settling Time	T_{settle}	–	16.5	20	µs	Time to settle to ±0.5% of frequency offset, as shown in Figure 29

8.4. Software OE Functional Description

Output driver can be enabled or disabled through control registers 0x01[10] (corresponding part number option should be selected to enable this function, please refer to the OE Pin Control option in Ordering Information section). To enable the output driver, this register should be set to 1, to disable – to 0.

Important note: By default (at startup) output is disabled in this mode and should be enabled by corresponding write operation after start-up.

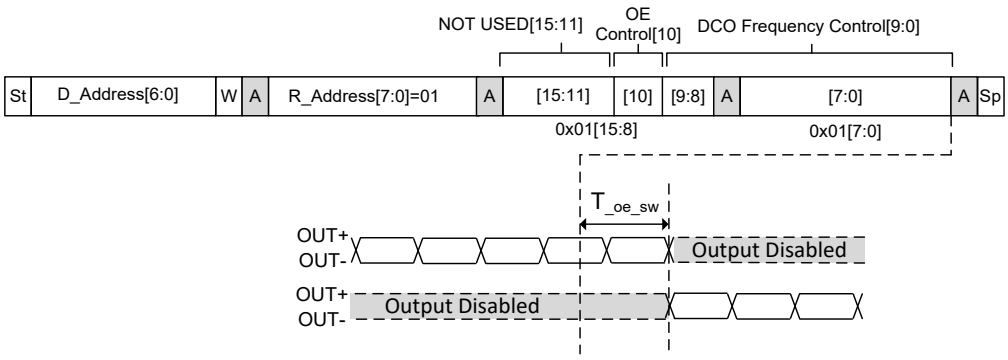


Figure 30. Enable/Disable software OE (I²C)

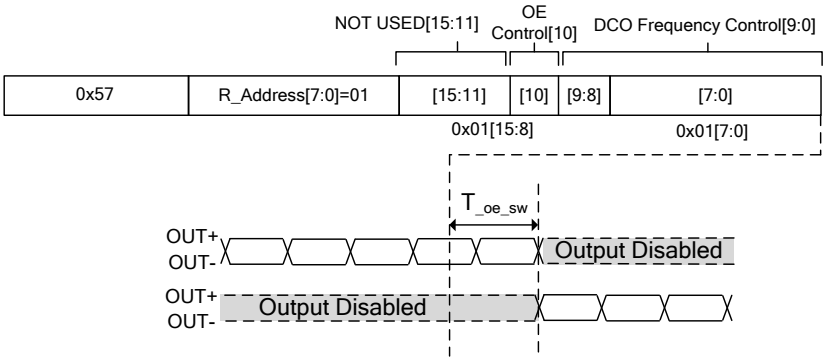


Figure 31. Enable/Disable software OE (I²C)

9 I²C/SPI Control Registers

The any-frequency, DCO software OE and drive strength control features enable control of frequency pull range, frequency pull value, Output Enable and Drive strength setting via I²C/SPI writes to the control registers.

Table 25 below shows the register map summary and the detailed register descriptions follow.

Table 25. Register Map Summary

Address	Bits	Access	Description
0x00	[15:0]	RW	DCO FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW)
0x01	[15:11]	R	NOT USED
	[10]	RW	OE CONTROL. This bit is only active if the output enable function is under software control. If the device is configured for hardware control using an OE pin, writing to this bit has no effect. Selection of Pin or Software OE Control is an ordering option shown in Ordering Information Table.
	[9:0]	RW	DCO FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW)
0x02	[15:4]	R	NOT USED
	[3:0]	RW	DCO PULL RANGE CONTROL
0x03	[15:11]	RW	FRAC-N PLL INTEGER DIVIDER
	[10:0]	RW	FRAC-N PLL FRACTIONAL DIVIDER, MOST SIGNIFICANT WORD (MSW)
0x04	[15:0]	RW	FRAC-N PLL FRACTIONAL DIVIDER, LEAST SIGNIFICANT WORD (LSW)
0x05	[15:3]	RW	POSTDIV
	[2:0]	RW	DRIVER CONTROL
0x06	[15:2]	R	NOT USED
	3	RW	MDRIVER DIVIDER VALUE
	[2:0]	RW	DRIVER CONTROL

Register Descriptions

9.1. Register Address: 0x00. DCO Frequency Control Least Significant Word (LSW)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	DCO FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW)[15:0]															

Bits	Name	Access	Description
15:0	DCO FREQUENCY CONTROL LEAST SIGNIFICANT WORD	RW	Bits [15:0] are the lower 16 bits of the 26 bit FrequencyControlWord and are the Least Significant Word (LSW). The upper 10 bits are in regsiter 0x01[9:0] and are the most significant Frequency Control Word (MSW). The lower 16 bits together with upper 10 bits specify a 26-bit frequency control word. This power up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After powerup, the system can write to these two registers to pull the frequency across the pull range. The register values are 2's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the next section.

9.2. Register Address: 0x01. OE Control, DCO Frequency Control Most Significant Word (MSW)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	NOT USED					OE	DCO FREQUENCY CONTROL[9:0] MSW									

Bits	Name	Access	Description
15:11	NOT USED	R	Bits [15:10] are read only and return all 0's when read. Writing to these bits have no effect.
10	OE Control	RW	Output Enable Software Control. Allows the user to enable and disable the output driver via I2C. 0 = Output Disabled (Default) 1 = Output Enabled This bit is only active if the output enable function is under software control. If the device is configured for hardware control using an OE pin, writing to this bit has no effect.
9:0	DCO FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW)	RW	Bits [9:0] are the upper 10 bits of the 26 bit Frequency Control Word and are the Most Significant Word (MSW). The lower 16 bits are in register 0x00[15:0] and are the least significant Frequency Control Word (MSW). Theses lower 16 bits together with upper 10 bits specify a 26-bit frequency control word. This power up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After powerup, the system can write to these two registers to pull the frequency across the pull range. The register values are 2's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the next section.

9.3. Register Address: 0x02. DCO PULL RANGE CONTROL

Bit	15	14	13	12	11	10	9	6	5	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	X[12]	X[12]	X[12]	X[12]
Name	NONE												DCO PULL RANGE CONTROL			

Note:

12. Default values are factory set but can be over-written after power-up.

Bits	Name	Access	Description
15:4	NONE	R	Bits [15:4] are read only and return all 0's when read. Writing to these bits have no effect.
3:0	DCOs PULL RANGE CONTROL	RW	Sets the digital pull range of the DCO. The table below shows the available pull range values and associated bit settings. The default value is factory programmed. **Bit** **3210** 0000: Not used 0001: Not used 0010: Not Used 0011: ±25 ppm 0100: ±50 ppm 0101: ±80 ppm 0110: ±100 ppm 0111: ±125 ppm 1100: ±150 ppm 1001: ±200 ppm 1010: ±400 ppm 1011: ±600 ppm 1100: ±800 ppm 1101: ±1200 ppm 1110: ±1600 ppm 1111: ±3200 ppm

9.4. Register Address: 0x03. Flac-N PLL Integer Value and Flac-N PLL Fraction MSW

Bit	15	14	13	12	11	10	9	6	5	6	5	4	3	2	1	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Name	Flac-N PLL INTEGER VALUE					Flac-N PLL FRACTION MSW										

Bits	Name	Access	Description
15:11	Flac-N PLL Integer Value	RW	Sets the integer value of the Flac-N PLL. The default value is factory programmed to correspond to the desired output frequency (hence the x notation in the default value field) and can be changed by the user after powerup.
10:0	Flac-N PLL Fractional Value, MSW	RW	Most Significant Word (MSW) of Flac-N PLL. The MSW comprises the upper 11 bits of the 27-bit control word. The default value is factory programmed to correspond to the desired output frequency (hence the x notation in the default value field) and can be changed by the user after powerup.

9.5. Register Address: 0x04. Flac-N PLL Fraction LSW

Bit	15	14	13	12	11	10	9	6	5	6	5	4	3	2	1	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Name	Flac-N PLL Fraction, LSW															

Bits	Name	Access	Description
15:0	Flac-N PLL Fraction Value, LSW	RW	Sets the Least Significant Word of the Flac-N PLL Fraction. The default value is factory programmed to correspond to the desired output frequency (hence the x notation in the default value field) and can be changed by the user after powerup.

9.6. Register Address: 0x05. PostDiv, Driver Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0
Name	PostDiv													Driver Control		

Bits	Name	Access	Description	
15:3	PostDiv	RW	PostDiv Value. The default value is factory programmed to correspond to the desired output frequency (hence the x notation in the default value field) and can be changed by the user after powerup. The PostDiv Value Range is [2:8191].	
s2:0	Driver Control	RW	LVDS or HCSL driver	
			Bit Value	Frequnecy range
			001	1 to 250 MHz
			000	250.000001 to 340 MHz
			LVPECL driver	
			Bit Value	Frequnecy range
			110	1 to 250 MHz
			101	250.000001 to 340 MHz

9.7. Register Address: 0x06. mDriver, Driver Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	NOT USED												mDriver	Driver Control		

Bits	Name	Access	Description	
15:2	NOT USED	R	Bits [15:3] are read only and return all 0's when read. Writing to these bits have no effect.	
3ss	mDriver	RW	mDriver divider value. DO NOT change this bit. Default value is 2 for SiT3521.	
			Bit Value	mDriver
			0	2 (default, DO NOT change)
			1	1 (bypass)
2:0	Driver Control	RW	LVDS or HCSL driver	
			Bit Value	Frequency range
			000	1 to 340 MHz
			LVPECL driver	
			110	1 to 340 MHz

10 I²C Operation

10.1. I²C protocol

Data valid

The SDA line must be stable during the high period of the SCLK. SDA transitions are allowed only during SCLK low level for data communication. Only one transition is allowed during low SCLK pulse to communicate one bit of data. Figure 32 shows the detailed timing diagram.

START and STOP conditions

The idle I²C bus state occurs when both SCLK and SDA are not being driven by any master and are therefore in a logic HI state due to the pull up resistors. Every transaction begins with a START (S) signal and ends with a STOP (P) signal. A START condition is defined by a high to low transition on the SDA while SCLK is high. A STOP condition is defined by a low to high transition on the SDA while SCLK is high. START and STOP conditions are always generated by master. This slave module also supports repeated START (Sr) condition which is same as START condition instead of STOP condition (Blue color line shows repeated START in Figure 33).

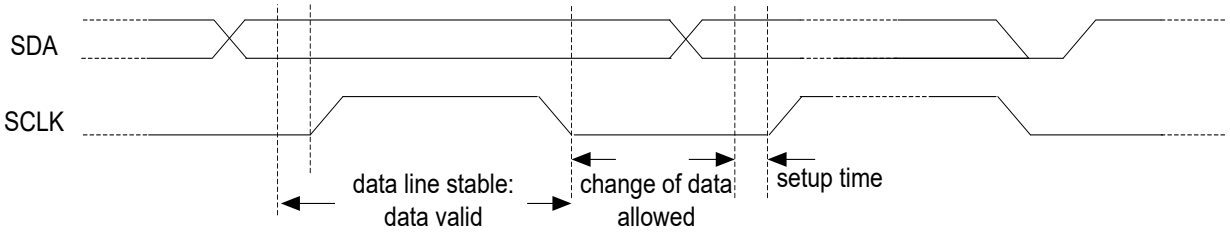


Figure 32. Data and clock timing relation in I²C bus

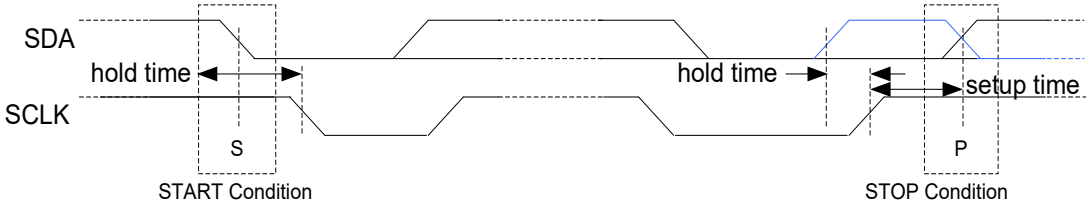


Figure 33. START and STOP (or repeated START) condition

Data Transfer Format

Every data byte is eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the MSB (Most Significant Bit) first. The detailed data transfer format is shown in Figure 34 below.

The acknowledge bit must occur after every byte transfer and it allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Setup and hold times must also be taken into account. When SDA remains high during this ninth clock pulse, this is defined as the Not-Acknowledge signal (NACK). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. The only condition that leads to the generation of NACK from the SiT3521 is when the transmitted address does not match the slave address. When the master is reading data from SiT3521, the SiT3521 expects the ACK from the master at the end of received data, so that the slave releases the SDA line and the master can generate the STOP or repeated START. If there is NACK signal at the end of data, then the SiT3521 tries to send the next data. If the first bit of next data is “0”, then the SiT3521 holds the SDA line to “0”, thereby blocking the master from generating a STOP/(re)START signal.

Write/Read sequence

This I²C slave module supports 7-bit device addressing format. The 8th bit is a read/write bit and “0” indicates a read transaction and a “1” indicates a write transaction. The register addresses are 8-bits long with an address range of 0 to 255 (00h to FFh). Auto address incrementing is supported which allows data to be transferred to contiguous addresses without the need to write each address beyond the first address. Since the maximum register address value is 255, the address will roll from 255 to back to 0 when auto address incrementing is used. Obviously, auto address incrementing should only be used for writing to contiguous addresses. The data format is

16-bit (two bytes) with the most significant byte being transferred first.

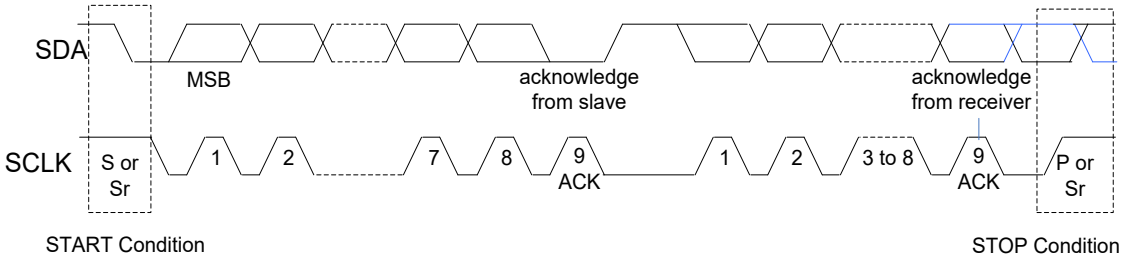


Figure 34. Data Transfer Format

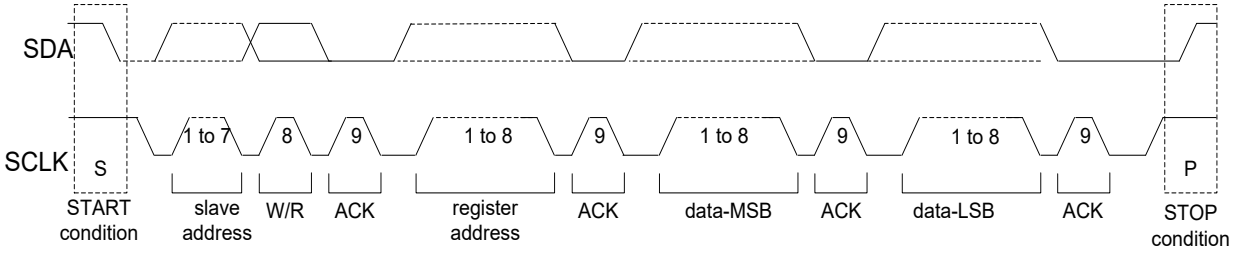


Figure 35. Write/Read Sequence

10.2. I²C Timing Specification

The below timing diagram and table illustrate the timing relationships for both master and slave.

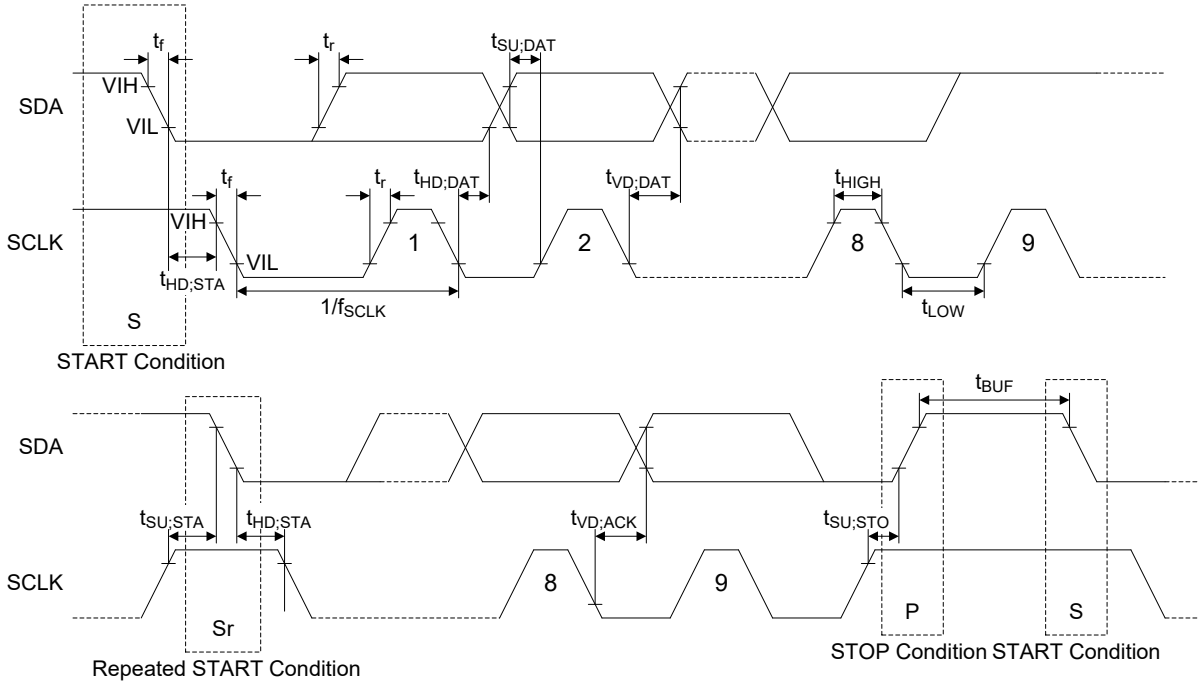


Figure 36. I²C Timing Diagram

Table 26. I²C Timing Requirements

All Min and Max limits are specified for Industrial Temperature range and over the rated operating voltage with 255 Ohm resistor and 550 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Parameter	Symbol	Standard mode			Fast mode			Fast mode plus [13]			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
SCLK clock frequency	f_{SCLK}	–	–	100	–	–	400	–	–	1000	kHz
Low period of SCLK clock	t_{LOW}	470	–	–	1300	–	–	500	–	–	ns
High period of SCLK clock	t_{HIGH}	400	–	–	600	–	–	260	–	–	ns
Rise time of both SCLK and SDA	t_r	–	–	120	–	–	120	–	–	120	ns
Fall time of both SCLK and SDA	t_f	30	–	300	30	–	300	30	–	120	ns
Hold time for Start condition	$t_{HD;STA}$	4000	–	–	600	–	–	260	–	–	ns
Setup time for Start condition	$t_{SU;STA}$	470	–	–	600	–	–	260	–	–	ns
Data setup time	$t_{SU;DAT}$	250	–	–	100	–	–	50	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	0	–	–	0	–	–	ns
Data valid time	$t_{VD;DAT}$	–	–	3450	–	–	900	–	–	450	ns
Data valid acknowledge time	$t_{VD;ACK}$	–	–	3450	–	–	900	–	–	450	ns
Setup time for stop condition	$t_{SU;STO}$	400	–	–	600	–	–	260	–	–	ns
I²C bus free time between stop and start	t_{BUF}	470	–	–	1300	–	–	500	–	–	ns

Notes:

13. Fast mode plus is not supported in Extended Industrial temperature range.

10.3. I²C Device Address Modes

There are two I²C Address modes:

1) Factory Programmed Mode. The lower 4 bits of the 7-bit device address are set by ordering code as shown in Table 27 below. There are 16 factory programmed addresses available. In this mode, pins 4 and 5 are NC and pin control of the I²C address is not available.
2) A0, A1 Pin Control. This mode allows the user to select between four I²C Device addresses as shown in Table 28.

Table 27. Factory Programmed I²C Address Control

I²C Address Ordering Code	Device I²C Address
0	1100000
1	1100001
2	1100010
3	1100011
4	1100100
5	1100101
6	1100110
7	1100111
8	1101000
9	1101001
A	1101010
B	1101011
C	1101100
D	1101101
E	1101110
F	1101111

Table 28 is only valid for the ordering option which does not use the I²C address pins A0, A1.

Table 28. Pin Selectable I²C Address Control

A1 Pin 4	A0 Pin 5	I²C Address
0	0	1100000
0	1	1100010
1	0	1101000
1	1	1101010

Ordering Information Table is only valid for the ISP-DCXO device option which uses pin control (A0, A1) of the I²C address. This mode corresponds to ordering code “G” in the I²C address section of the ordering code table.

11 SPI Operation

SPI (Serial Peripheral Interface) is a 4-pin synchronous serial protocol that allows a master device to initiate half-duplex communication with one or more slave devices. The pin functions are as follows:

SCLK: Serial Clock which supports up to 5 MHz operating frequency.

MOSI: Master Output Slave Input. This is the data input pin to the SiT3521 and is used by the master to write data to the SiT3521 control registers.

MISO: Master Input Slave Output. This is the data output pin of the SiT3521 and is used by the master to read data from the SiT3521 control registers.

$\overline{SS}$: Active Low SPI Chip Select. This pin is used by the master to select the SiT3521 as the active slave device on the SPI bus. When the master drives the SiT3521 pin low, the SiT3521 is selected as the target of a read or write transaction.

The following Figure 37 illustrates the logical connection between one SPI master and 3 SPI slaves. Note that this diagram is shows only an example logical connection and is not a detailed schematic intended to show pull-up resistors and other components which may also be required.

There are two allowed states for idle SCLK state, HI and LOW and these states are called clock phase. There are also two modes for clock sampling edge, rising edge and falling edge and these modes are called clock polarity. Since there are two allowed clock phases and two allowed clock polarities, this means there are four total modes of SPI operation as illustrated below in Figure 38.

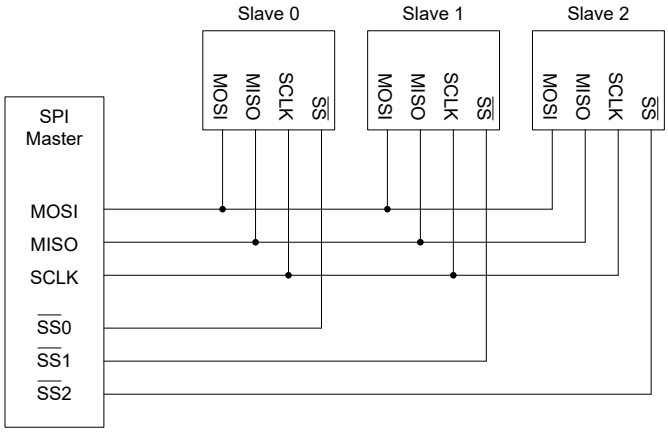


Figure 37. Multi-slave SPI bus connections

Mode	SCLK Polarity SCLK_POL	SCLK Phase SCLK_PHA
Mode 0	Low At Start	Rising Edge
Mode 1	Low At Start	Falling Edge
Mode 2	High At Start	Falling Edge
Mode 3	High At Start	Rising Edge

Figure 38. SPI operation modes

The SiT3521 can support all four operating modes. By default, modes 0 and 3 are supported, but modes 1 and 2 can be supported in the future.

The serial byte interface format is shown below: 8-bit command (read or write), 8-bit SPI address and 16-bit data.

The serial order is most significant bit (MSB) first. The SPI protocol also supports auto address incrementing which means the address will automatically increment after the first transaction. Auto address incrementing will result in higher data throughput when writing to registers with contiguous addresses. If it is required to write to non-contiguous addresses, a write command and register address must be used for each transaction after the delay (125 us min). Without such delay, the device will consider command and address bytes as a data for the consequent register.

The detail register descriptions are covered in the I2C/SPI Control Registers.

A description of DCO control is in DCO Functional Description and a description of changing the output center frequency is in any-frequency Functional Description.

The below Figure 40 shows the timing diagram for modes 0 and 3.

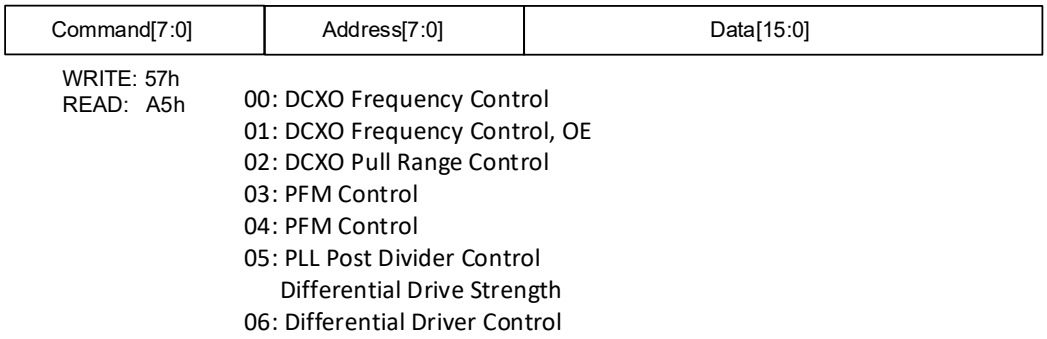


Figure 39. SPI control word format

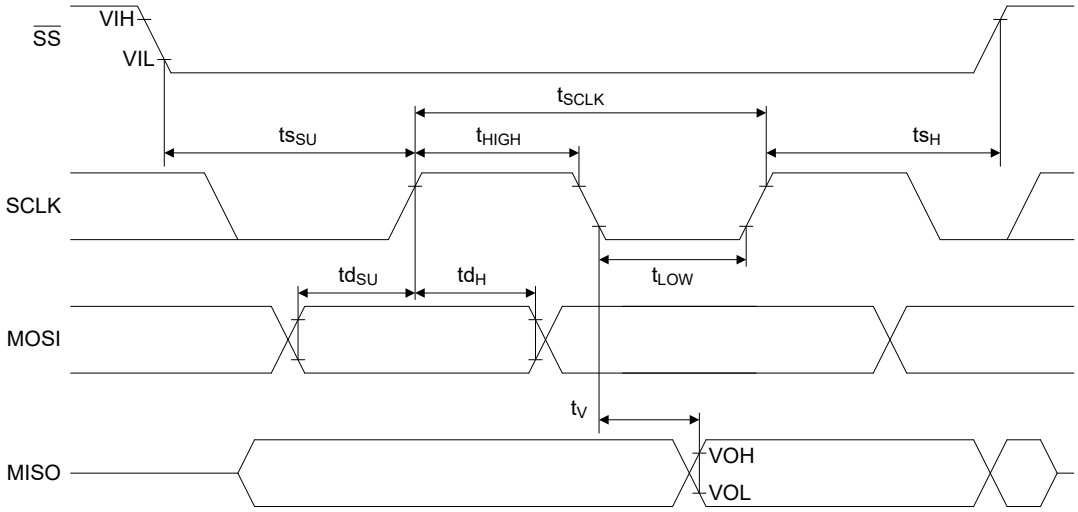


Figure 40. SPI Timing Diagram (Mode 0/3)

Table 29. SPI Timing Requirements[14]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Setup time for MOSI to SCLK Rising Edge	td_{SU}	28	–	–	ns
Hold time for MOSI to SCLK Rising edge	td_H	1	–	–	ns
Time from active edge of SCLK clock to valid MISO data available at pin	t_v	–	–	30	ns
Period of SCLK	t_{SCLK}	–	–	200	ns
High Width of SCLK	t_{HIGH}	–	$t_{SCLK}/2$	–	ns
Low Width of SCLK	t_{LOW}	–	$t_{SCLK}/2$	–	ns
Setup time for SSB falling edge to SCLK rising edge	ts_{SU}	$1.5*t_{SCLK}$	–	–	ns
Hold time from SSB rising edge to SCLK rising edge	ts_H	$1.5*t_{SCLK}$	–	–	ns

Notes:

14. SPI is not supported in Extended Industrial temperature range.

Schematic Examples

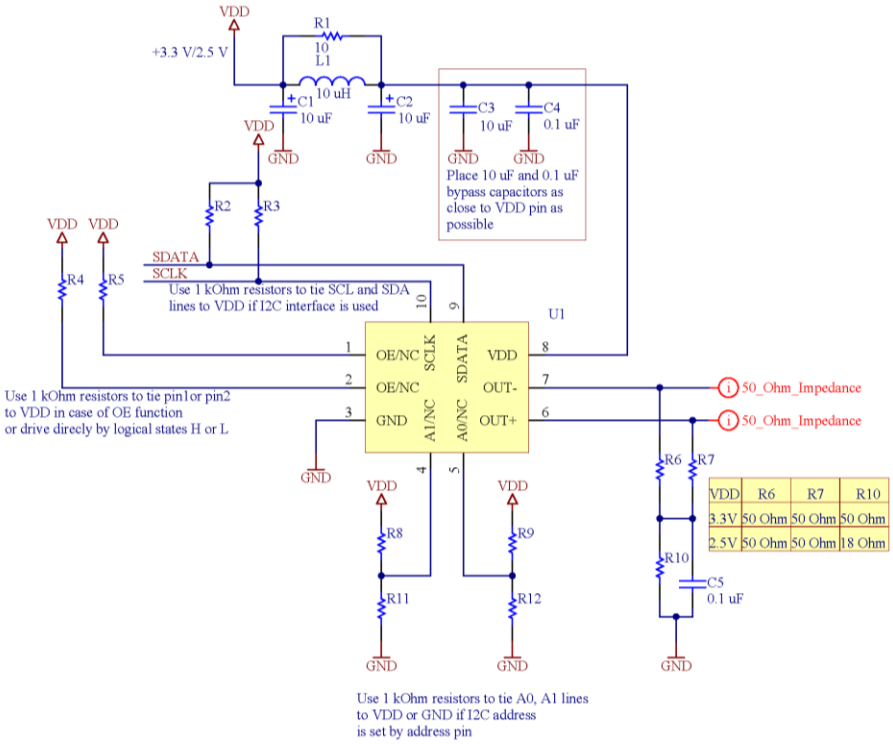


Figure 41. Schematic Example (LVPECL, I²C mode)

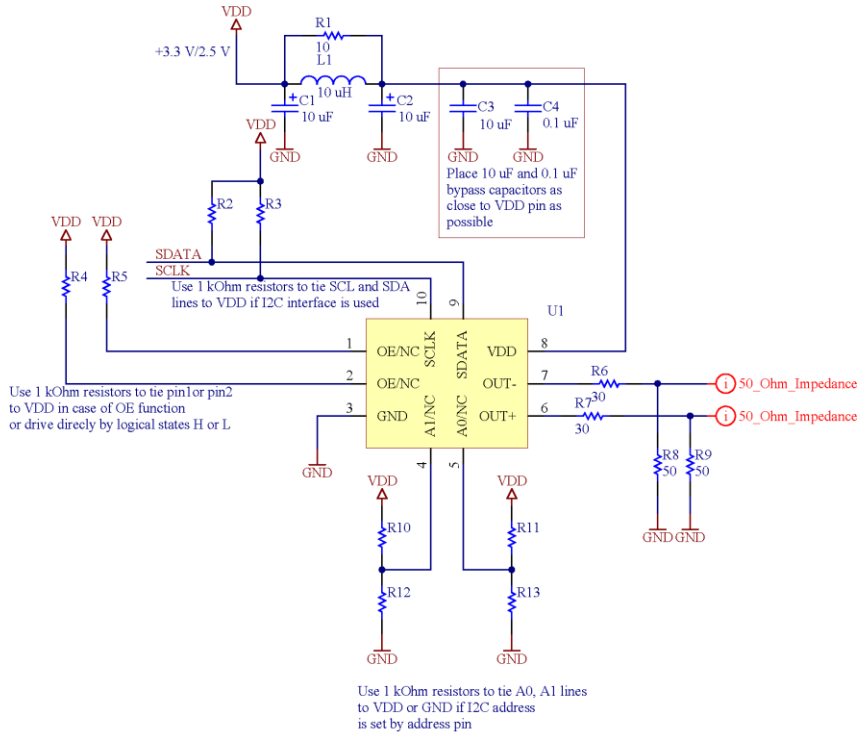


Figure 42. Schematic Example (HCSL, I²C mode)

Schematic Examples (continued)

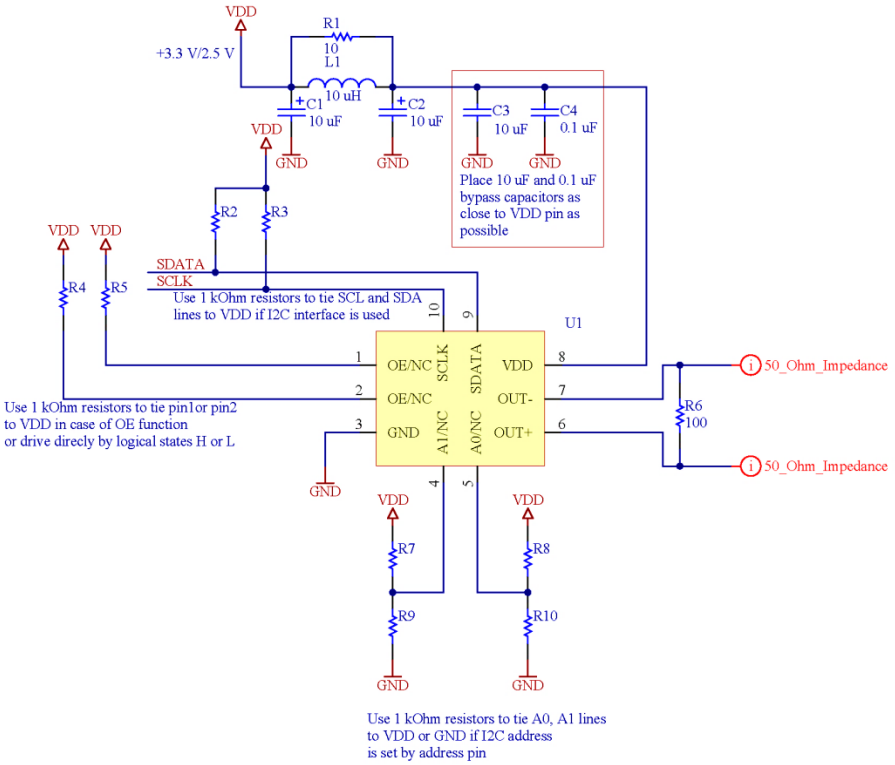


Figure 43. Schematic Example (LVDS, I²C mode)

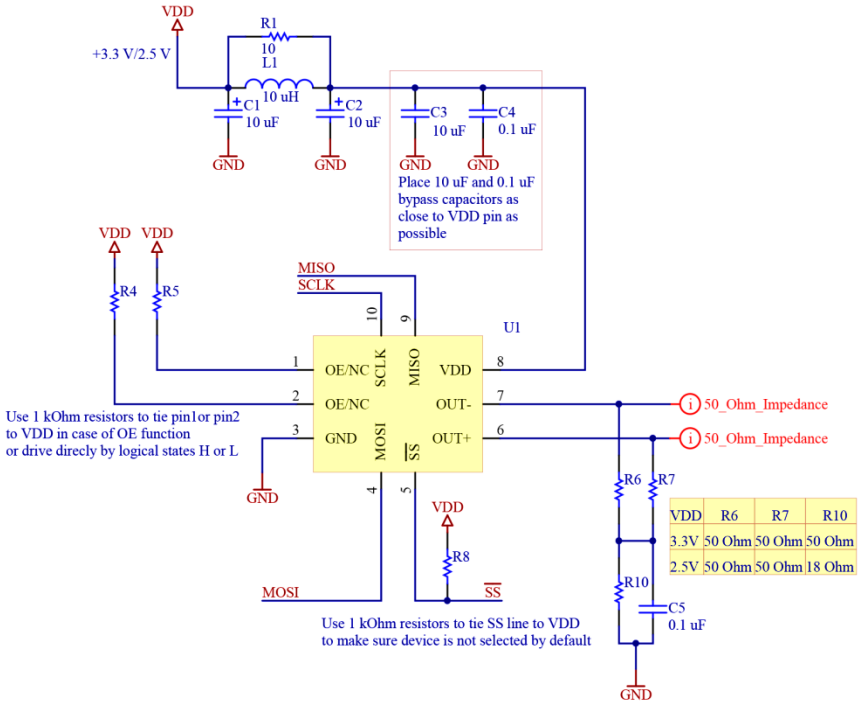


Figure 44. Schematic Example (LVPECL, SPI mode)

Schematic Examples (continued)

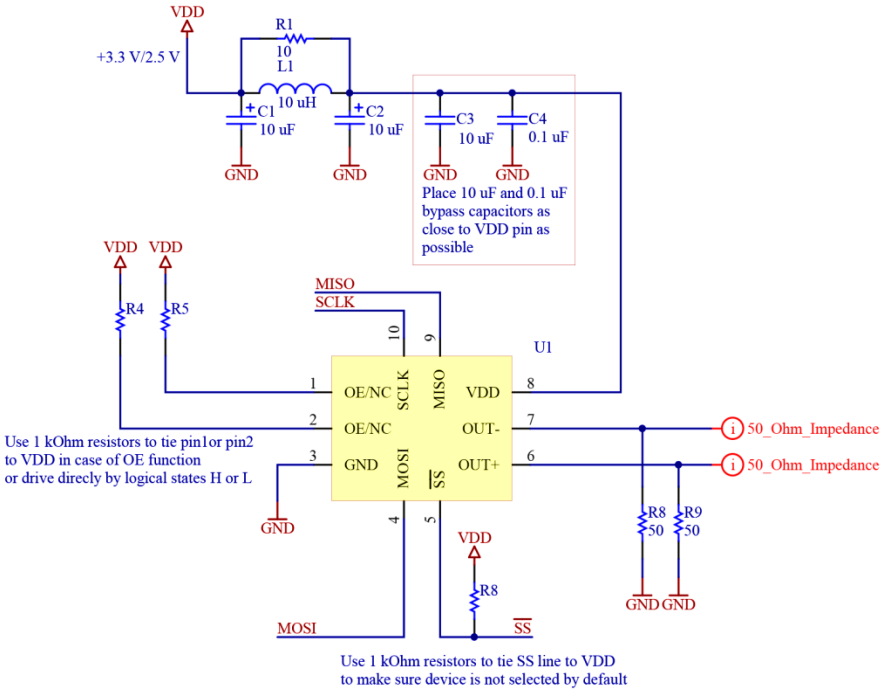


Figure 45. Schematic Example (HCSL, SPI mode)

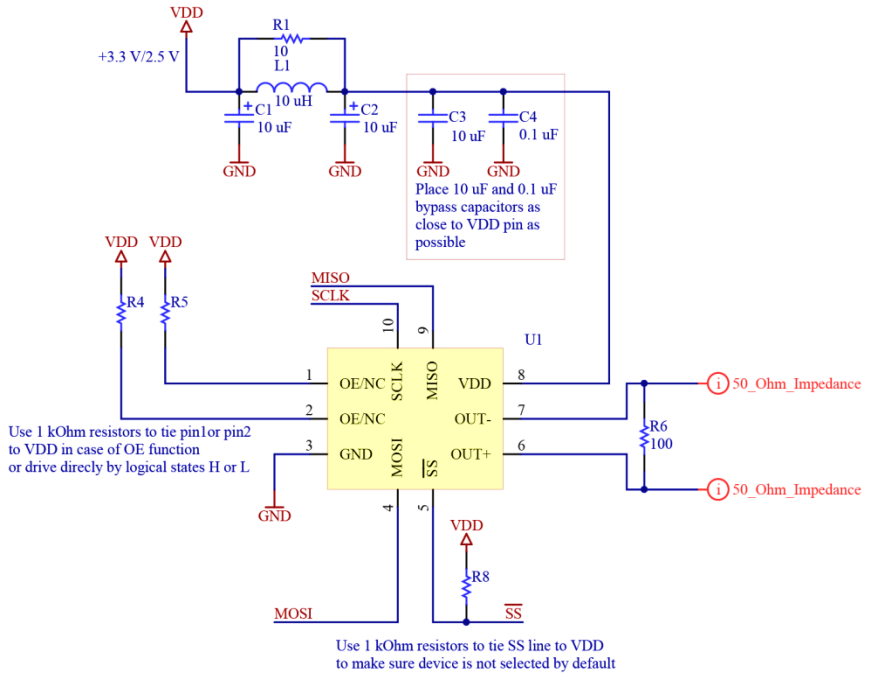
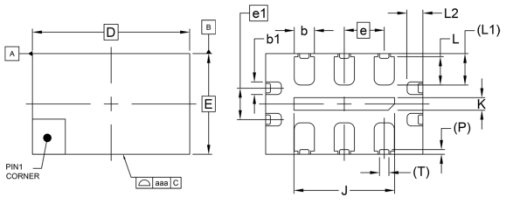


Figure 46. Schematic Example (LVDS, SPI mode)

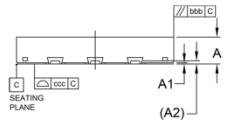
Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[15]	Recommended Land Pattern (Unit: mm)[16]

5.0 x 3.2 x 0.85 mm



TOP VIEW BOTTOM VIEW



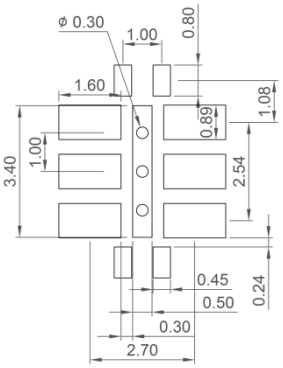
SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		5.000 BSC	
	Y	E		3.200 BSC	
EP SIZE	X	J	3.100	3.200	3.300
	Y	K	0.300	0.400	0.500
LEAD WIDTH		b	0.590	0.640	0.690
		b1	0.350	0.400	0.450
LEAD LENGTH		L	0.850	0.900	0.950
		L1		1.000 REF	
		L2	0.450	0.500	0.550
LEAD PITCH		e		1.270 BSC	
		e1		1.000 BSC	
PACKAGE TOLERANCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANRITY		ccc		0.080	
DIMPLE WIDTH		T		0.300 REF	
DIMPLE LENGTH		P		0.150 REF	
DIMPLE DEPTH		A2		0.100 REF	

NOTES

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.

Package Outline	
10L PQFV	POD-PQFV-010-C05032-040
5.0 x 3.2 x 0.85 mm	SiTime
2019/03/13	



Solder Print Layout	
10L QFN	SPL-001-RevA
5.0 x 3.2 x 0.85 mm	SiTime
2017/11/29	

Notes:

15. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
16. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Additional Information

Table 30. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Part number Generator	Tool used to create the part number based on desired features.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	http://www.sitime.com/manufacturing-notes
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
Time Master Web Based Configurator	Tool to establish proper programming	https://www.sitime.com/time-master-web-based-configurator
Evaluation Boards	SiT6712EB Evaluation Board User Manual	https://www.sitime.com/support/user-guides
Demo Boards	SiT6701DB, SiT6702DB Demo Board User Manual	https://www.sitime.com/support/user-guides

Revision History

Table 31. Revision History

Revisions	Release Date	Change Summary
0.1	03/03/2017	Initial draft
0.2	03/10/2017	Added I²C Timing diagram for ISP Function
		Modified Block Diagram to include approximate MEMS frequency (47 MHz)
		Updated ISP function procedure
		Updated Package Drawing
0.21	03/10/2017	Added Table 5, I²C Electrical Characteristics
0.22	10/11/2017	Fixed I²C Timing diagram on page 12 to show output disabled when first PFM value is written.
		Added Output Drive Strength Control to Block Diagram on page 9
		Changed PFM Range from 12.59 - 16.34 to 13.83 – 15.43. Changed 156.25 MHz programming example so that it corresponds to the new PFM range. Updated logo and company address, other page layout changes
0.90	04/02/2018	Preliminary release
0.99	08/22/2018	Updated thermal numbers, fixed minor errors
0.991	04/25/2020	±10 ppm option Updated POD (Dimensions Drawings) Added Evaluation and Demo Boards reference in Additional Information Other page layout changes Added HTS classification code Added 105°C support for I2C operation Increased max operating junction temperature for 70°C and 85°C ambient Updated Frac-N PLL numbers in Table 19 Updated I2C Timing Requirements for “Fall time of both SCLK and SDA”

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439